ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
www.adsantec.com

ASNT2123-KMM-Evaluation Board
60*Gbps* 4:1 Digital DeMux
Application Note

Overview

ASNT2123-KMM is a low power and high-speed digital 1-to-4 deserializer-demultiplexer (DMUX) that functions seamlessly over data rates (*f*bit) ranging from DC to its maximum speed.
The main function of the part is to demultiplex an incoming high speed serial differential CML data bit stream dp/dn running at a bit rate of *f*bit into 4 parallel data channels q0p/q0n, q1p/q1n, q2p/q2n, q3p/q3n running at a bit rate of *f*bit/4. Differential or single-ended half-rate clock cep/cen must be provided by an external source for the part to function properly.
The parallel words and clock divided-by-4 c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in a very little relative skew over the operating temperature range of the device. The evaluation board operates from a -3.3*V* power supply.

Evaluation board

ADSANTEC's evaluation board contains fourteen edge mount male SMP full detent Fairview connectors MFG PN: SC5382, 50*Ohm* transmission lines to the device, and power supply decoupling networks on the evaluation board. It measures approximately 2 x 2 inches, with connectors. A MOLEX connector MFG PN: 39-28-1023 is used to supply power. **Figure 1** shows the evaluation board with corresponding connections for operation.

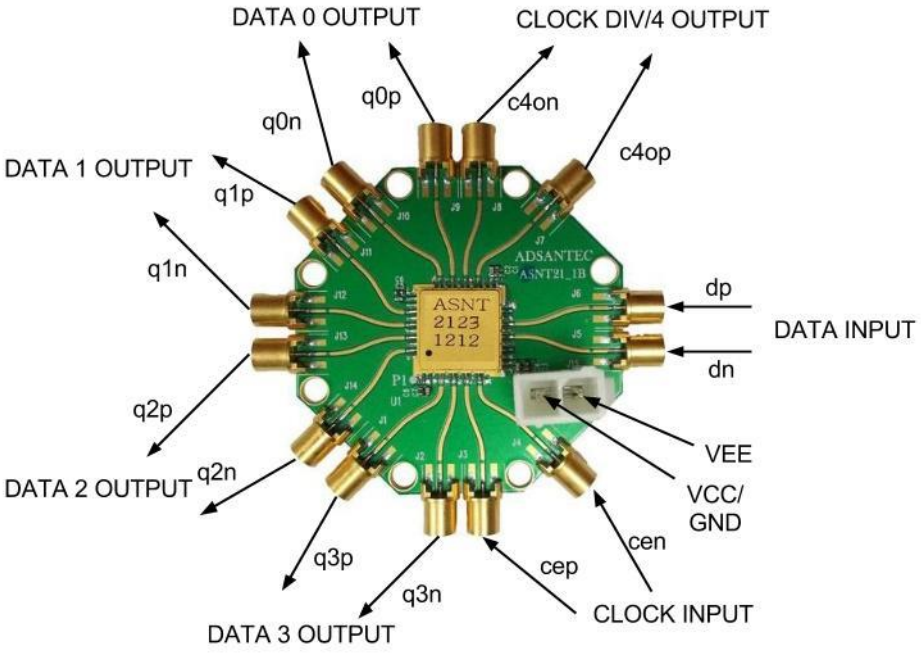

Figure 1. Pin Description

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275
Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
www.adsantec.com

Operation

1. The part is static sensitive. Please observe anti-static protection procedures!
2. The ground plane on the PCB shown in **Figure 1** is connected to vcc. The description of all connectors is presented in Table 1.
3. Switch on an external power supply unit and set it to a negative supply voltage with the value of -3.3*V* (positive output pin of the unit must be shorted to ground). Connect this power supply to the vee connector.
4. Differential data inputs dp/dn are designed for CML-type signals and have on-chip 50*Ohm* terminations from the corresponding pins to vcc. Single-ended or differential input signals may be applied AC-coupled or DC-coupled. In case of DC-coupling, make sure that the input data's common mode voltage is within the specified range (see the Datasheet for more details).
5. Differential clock inputs cep/cen are designed for CML-type signals and have on-chip 50*Ohm* terminations from the corresponding pins to vcc. Single-ended or differential input signals may be applied AC-coupled or DC-coupled. In case of DC-coupling, make sure that the input data's common mode voltage is within the specified range (see the Datasheet for more details).
6. Low-speed divided-by-4 differential clock outputs c4op and c4on deliver CML-type signals and have on-chip 50*Ohm* terminations from the corresponding pins to vcc. They also require an external 50*Ohm* termination to vcc. These outputs can be directly connected to an oscilloscope or to any CML inputs with internal 50*Ohm* termination to vcc (ground plane). AC coupling is also acceptable.
7. Differential data outputs q0p/q0n, q1p/q1n, q2p/q2n, and q3p/q3n deliver CML-type signals and have on-chip 50*Ohm* terminations from the corresponding pins to vcc. They also require an external 50*Ohm* termination to vcc. These outputs can be directly connected to an oscilloscope or to any CML inputs with internal 50*Ohm* termination to vcc (ground plane). AC coupling is also acceptable.
8. After the part's activation, all signals can be applied or disconnected without the removal of the power supply voltage.

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275
Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
www.adsantec.com

Table 1. Signal Connectors.

Symbol	Signal description	On-chip name	Polarity	I/O type
J6	Data input	dp	Direct	CML-type input with on-chip 50*Ohm* termination to vcc
J5		dn	Inverted	
J3	Half-rate clock input	cep	Direct	CML-type input with on-chip 50*Ohm* termination to vcc
J4		cen	Inverted	
J9	Data output 0	q0p	Direct	CML-type output with on-chip 50*Ohm* termination to vcc
J10		q0n	Inverted	
J11	Data output 1	q1p	Direct	CML-type output with on-chip 50*Ohm* termination to vcc
J12		q1n	Inverted	
J13	Data output 2	q2p	Direct	CML-type output with on-chip 50*Ohm* termination to vcc
J14		q2n	Inverted	
J1	Data output 3	q3p	Direct	CML-type output with on-chip 50*Ohm* termination to vcc
J2		q3n	Inverted	
J7	Clock divided by 4 output	c4op	Direct	CML-type output with on-chip 50Ohm termination to vcc
J8		c4on	Inverted	
J15	Negative supply voltage	vee		DC power supply

REVISION HISTORY

Revision	Date	Changes
1.0.1	11-2013	Initial release