ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
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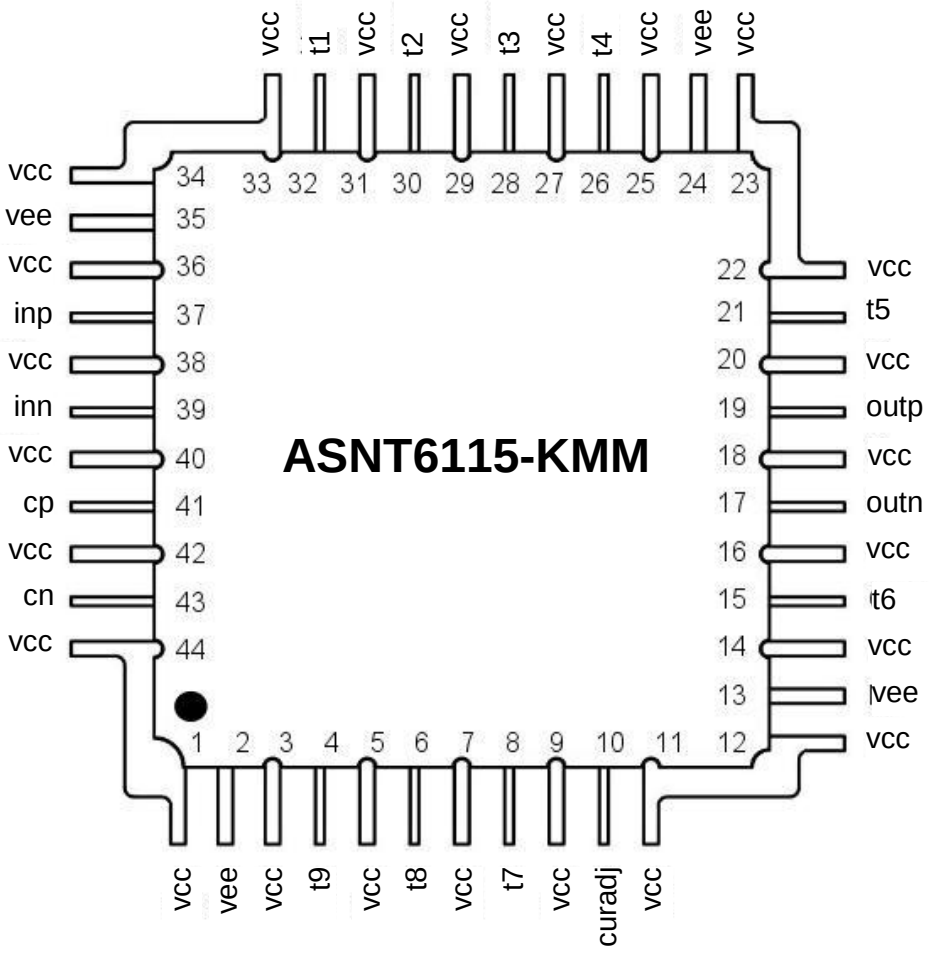
ASNT6115-KMM
5.6*GHz* Finite Impulse Response Filter

- DC to 5.6*GHz* finite impulse response filter.
- Two differential CML-type input ports and one differential CML-type output port.
- Nine analog tap-weight control inputs.
- Differential gain of approximately 0*dB*.
- Single +3.3*V* or -3.3*V* power supply.
- Power consumption: 422*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 44-pin package.



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DESCRIPTION

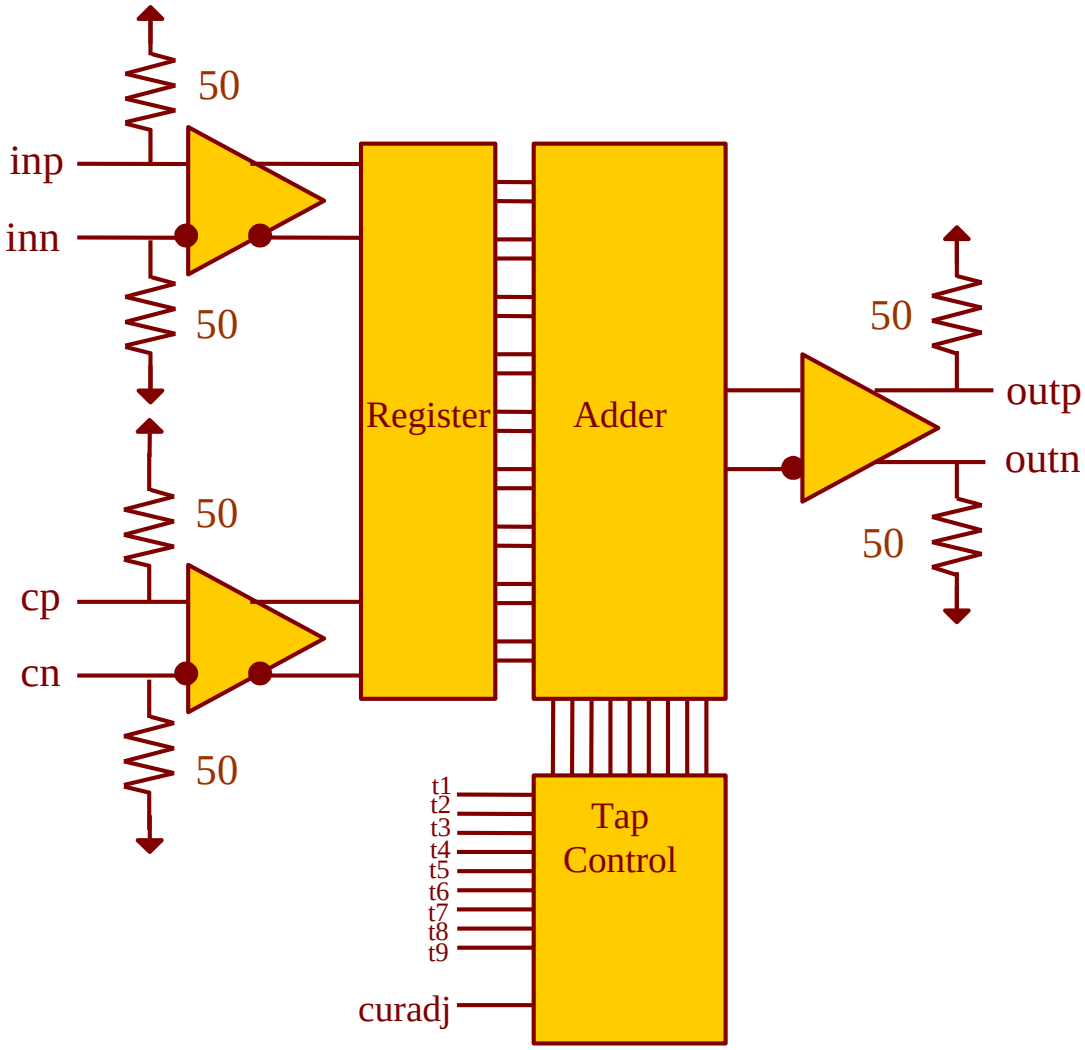

Fig. 1. Functional Block Diagram.

The IC shown in Fig. 1 receives a data signal with the rate of up to 5.6*Gbps* through differential port inp/inn and a clock signal with the frequency of up to 5.6*GHz* through differential port cp/cn. The signals are used by the Register to generate 9 copies of the input data signal shifted by ½ of the clock period. Those 9 copies are linearly summed in the Adder with different weights and polarities that are externally controlled through the Tap Control's input single-ended ports t1/t2/t3/t4/t5/t6/t7/t8/t9. The resulting signal with the required digital pre-emphasis is supplied to the differential output (outp/outn) through a linear output buffer.

The input and output signals of the register are presented in Fig. 2.

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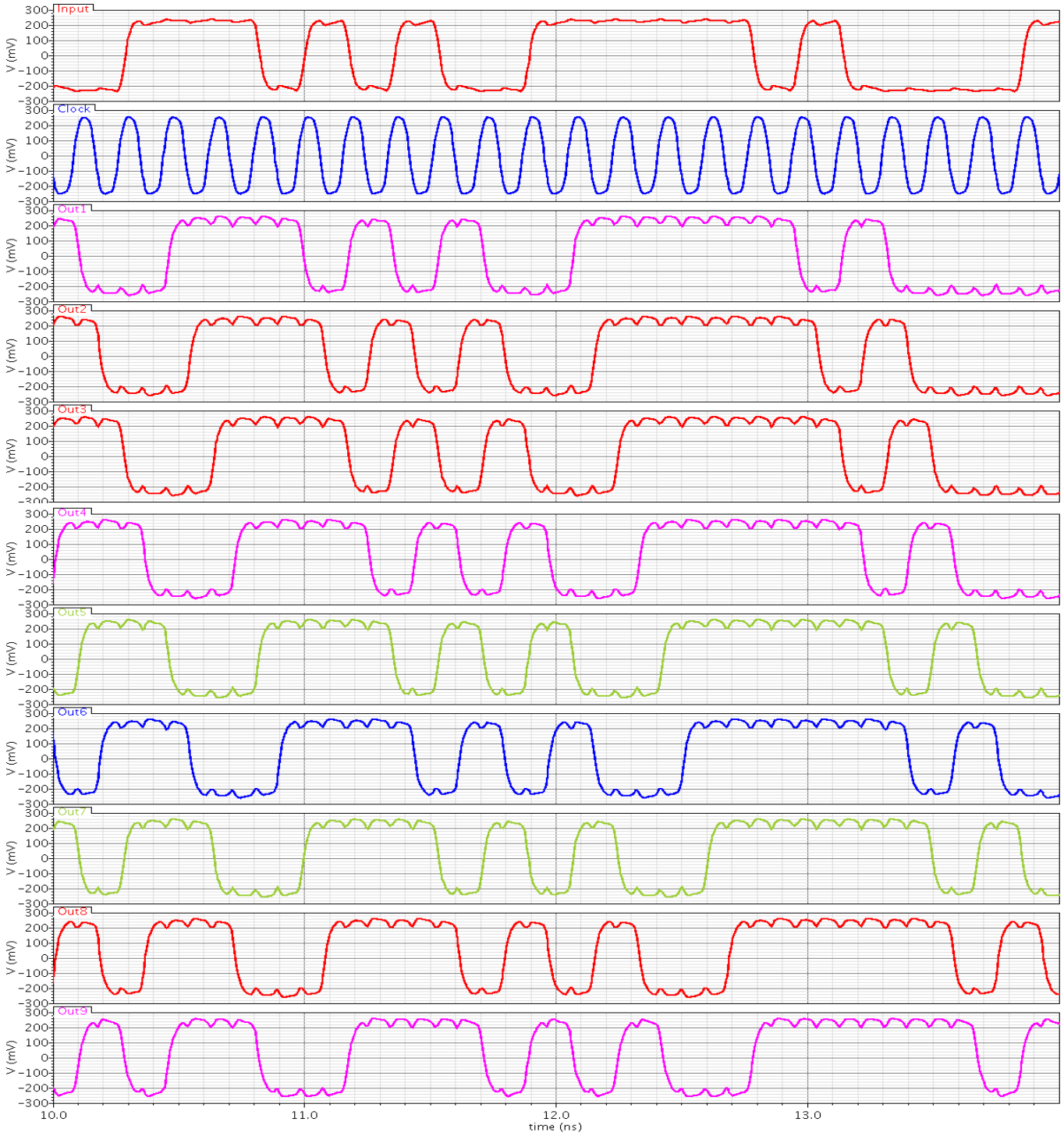

Fig. 2. Register Timing Diagram, 5.6GHz Clock.

The weight and polarity of each tap are set by the voltage on the corresponding input control port t1-t9. The dependence of the tap's current value and polarity on the input control voltage are presented in Fig. 3 and Fig. 4. The voltages below the threshold (approximately vcc-0.6*V*) correspond to negative currents while the voltages above the threshold correspond to positive currents.

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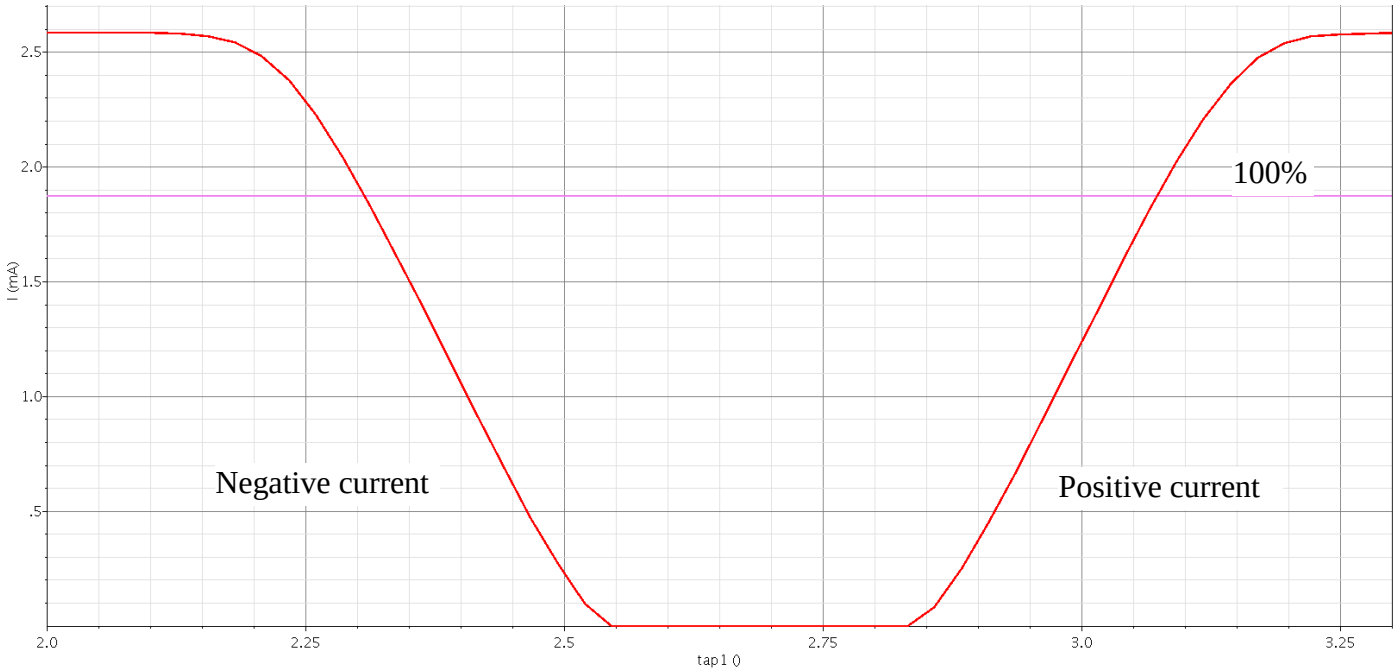

Fig. 3. Current of a Single Tap vs. Control Voltage

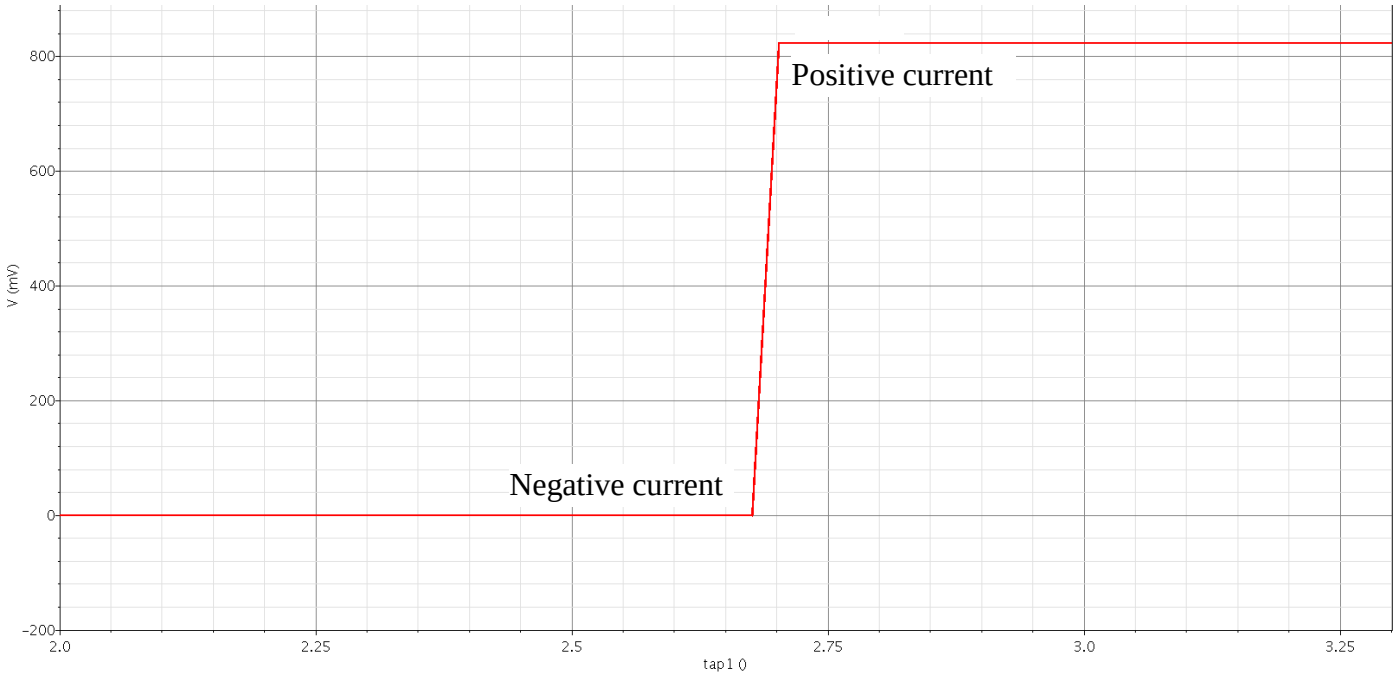

Fig. 4. Tap Phase vs. Control Voltage

Each tap control port generates a positive or negative tap current with the value from 0% to 100% of the maximum output current value *Imax* that is defined by the curadj control voltage as shown in Fig. 5.

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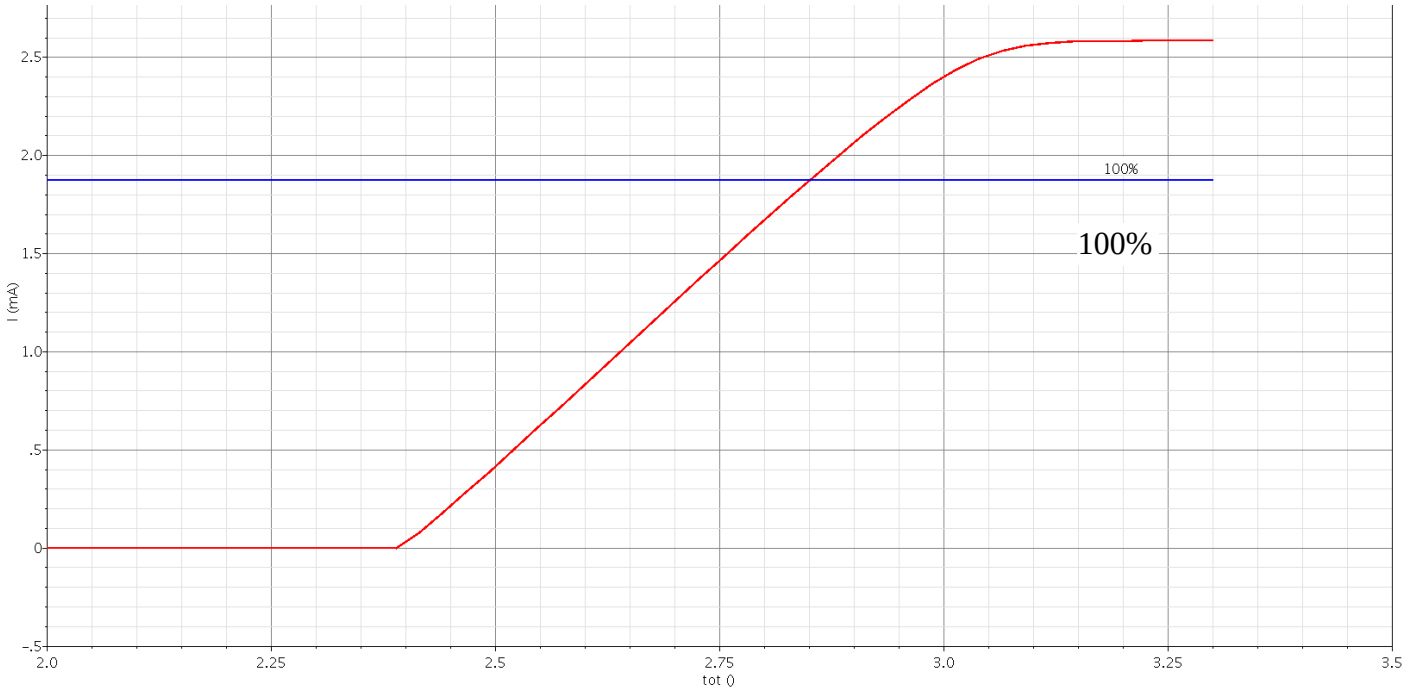

Fig. 5. Current of a Single Tap vs. curadj Voltage

To achieve the required output signal amplitude of *M*[%] of the maximum value independent from the tap control settings, the value of curadj should be set in accordance with the equation:

$$curadj[\%] = \frac{100 \cdot M[\%]}{\sum_{i-1}^{i=9} |t_i[\%]|} .$$

As can be seen from the graphs above, all controls cover a range from 0% to about 130% in order to ensure the linear control characteristics within the operational region.

The part's output buffers support the CML-type interface with on chip 50*Ohm* termination to vcc and may be used in either DC or AC coupling modes (see also POWER SUPPLY CONFIGURATION). The differential DC signaling is recommended for the optimal performance.

The part's input buffer supports the CML-type interface with equivalent on-chip 50*Ohm* termination and can be used in either DC or AC coupling modes. In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The differential signaling is recommended for the optimal performance.

POWER SUPPLY CONFIGURATION

IC can operate with either negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Supply Voltage (vee)		-3.5	*V*
Power Consumption		422	*mW*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
inp	37	CML input	Differential data inputs with internal SE 50*Ohm* termination to vcc.
inn	39		
cp	41	CML input	Differential clock inputs with internal SE 50*Ohm* termination to vcc.
cn	43		
outp	19	CML output	Differential data outputs. Require external SE 50*Ohm* termination to vcc.
outn	17		
t1	32	Analog input	Tap adjustment inputs that control tap weights and tap phases.
t2	30		
t3	28		
t4	26		
t5	21		
t6	15		
t7	8		
t8	6		
t9	4		
curadj	10	Analog input	Controls total current of all taps.

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply. (0*V* or -3.3*V*)	2, 13, 24, 35

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		128		*mA*	
Power consumption		422		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (d)					
Data Rate	0		5.6	*Gbps*	
CM Voltage Level	vcc -0.6	vcc -0.5	vcc +0.4	*V*	
HS Input Clock (c)					
Clock Rate	0		5.6	*GHz*	
CM Voltage Level	vcc -0.6	vcc -0.5	vcc +0.4	*V*	
HS Output Data (q)					
Optimal Amplitude		330		*mV*	Differential
CM Level		vcc -0.4		*V*	With external 50*Ohm* DC termination

PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin CQFP package shown in Fig. 1. The package's mechanical information is available on the company's website. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to vcc plain that is ground for the negative supply or power for the positive supply.

The package's leads will be trimmed to a length of 1.0*mm*. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   3.9.1 Solderability
   3.2.2 Solder Purity Maintenance
   3.9.2 Solderability Maintenance
   3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder.

The part's identification label is ASNT6112-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

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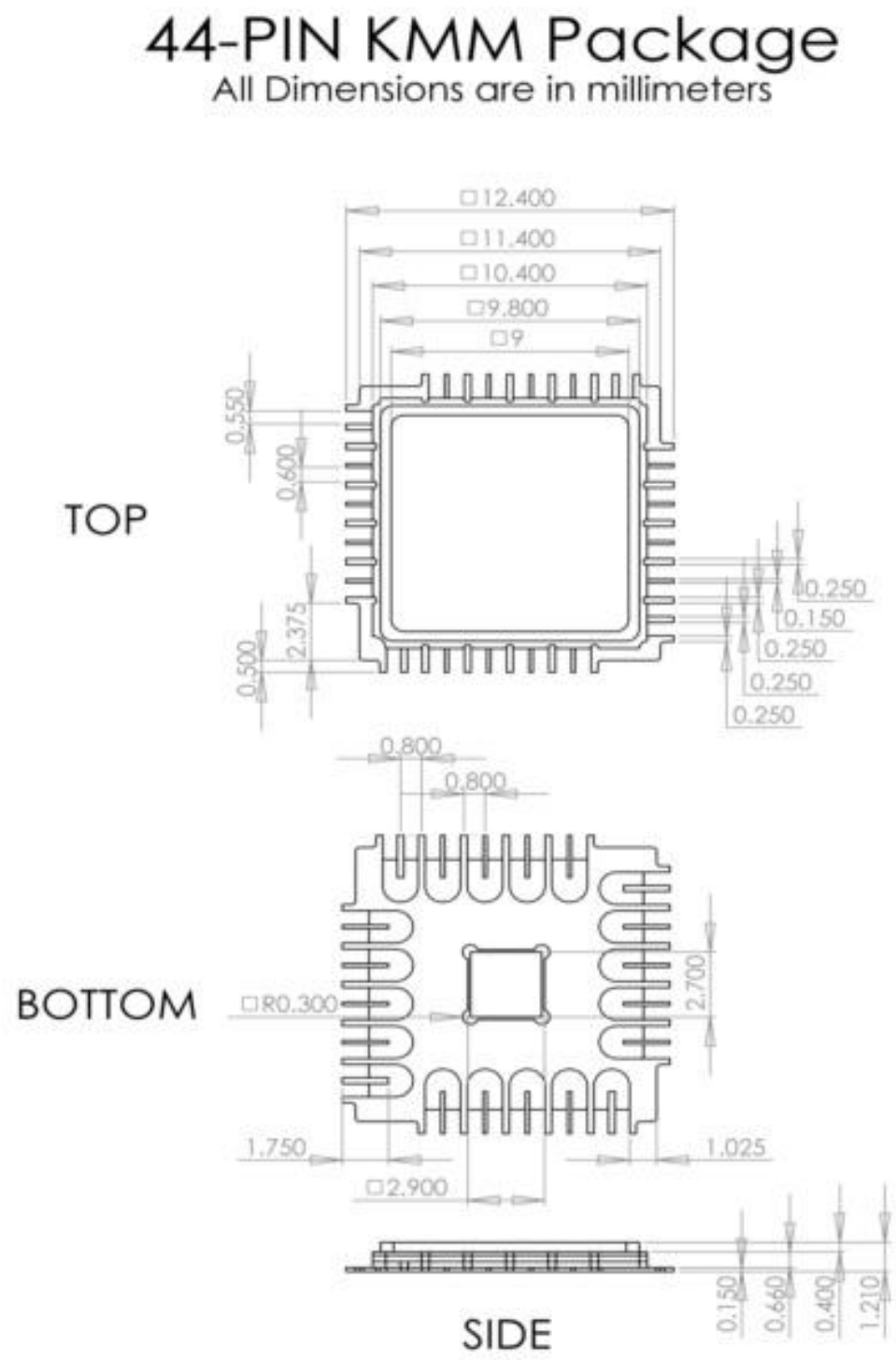

Fig. 1. Package Drawing.

REVISION HISTORY

Revision	Date	Changes
1.0.1	4-2012	Initial Release