ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

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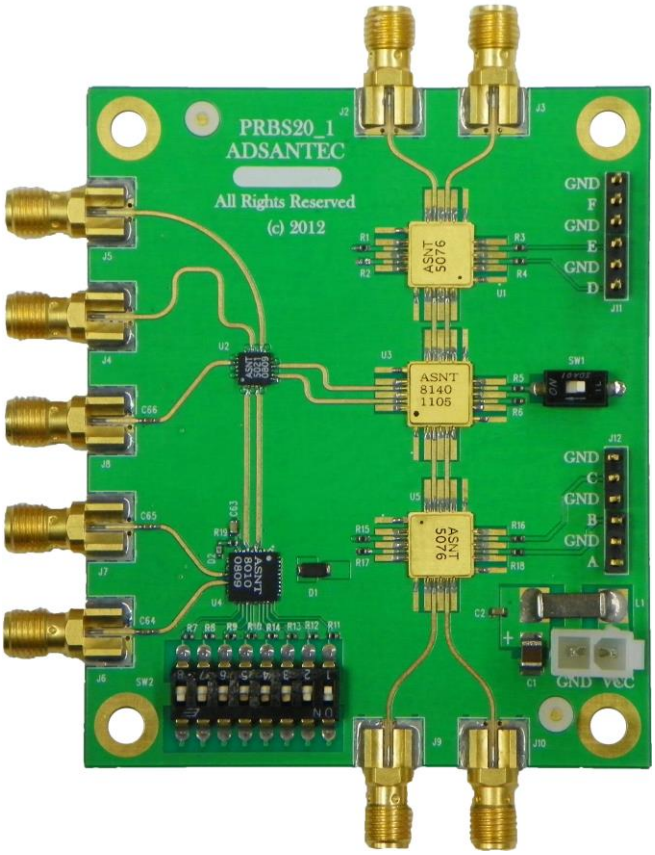
ASNT_PRBS20_1
18*Gbps* 2^7-1 PRBS Generator featuring Jitter Insertion, Selectable Sync, and Output Amplitude Control

- Broadband frequency range from 20*Mbps* – 18*Gbps*
- Minimal insertion jitter
- Fast rise and fall times
- Two PRBS data outputs
- Jitter insertion capability
- Output amplitude control from 0*V* to 1*V* peak to peak
- Up to 140*ps* delay variation on each output
- Buffered differential clock output
- 50% duty cycle for sync output on all divide ratios
- Sync output and Clock input are AC coupled on board
- Single +3.3*V* supply



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DESCRIPTION

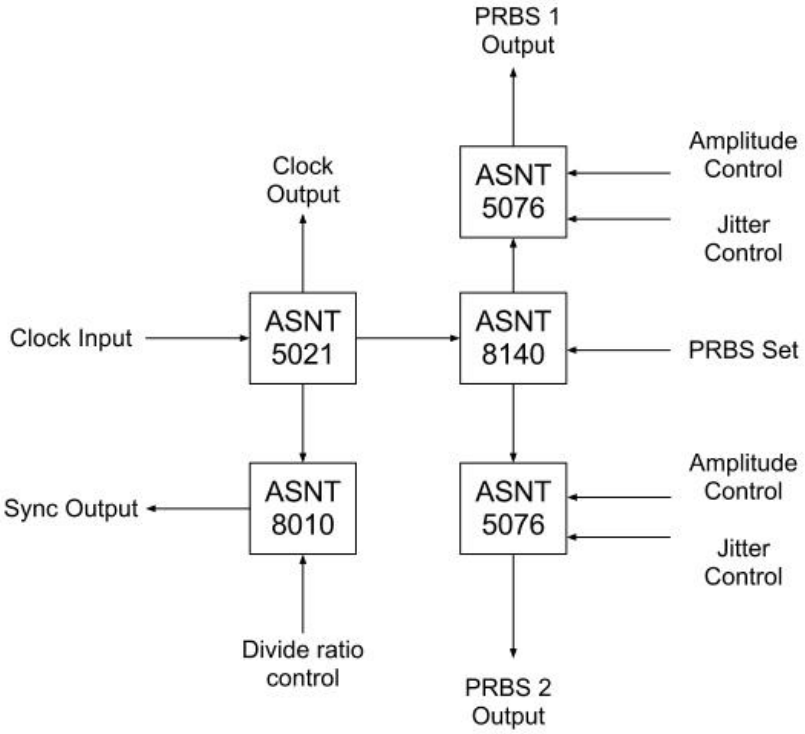

Fig. 1. Functional Block Diagram

The ASNT_PRBS20_1 is a broadband 2^7-1 PRBS generator intended for test, prototyping, microwave, and communication applications. The amplitude and phase can be individually adjusted on both differential outputs. Jitter can be inserted onto either differential output with a bandwidth up to 500*kHz*. The output amplitude on both PRBS outputs can be varied from 0*V* to 1*V* single-ended peak to peak. A single-ended clock from 10*MHz* to 18*GHz* with an amplitude as low as 50*mV* peak to peak may be applied to the clock input. A buffered differential clock output is provided on the board. A differential Sync Output divides an input clock from 1 to 256. The Sync Output is capable of displaying an eye diagram at divide-by-16 and a PRBS waveform output for 127 or 254. An on-board PRBS reset switch is present and should be used to preset the generator to avoid the all zero state lock-up.

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SYNC OUTPUT

The Sync Output can be configured to output any divide ratio from 1 to 256 from the clock input. It contains eight switches that represent 8 bits. The LSB starts at SW1 and the MSB ends at SW8. The binary value of zero gives a decimal n value of 256. Increasing binary values increases the decimal value of n as shown in Table 1.

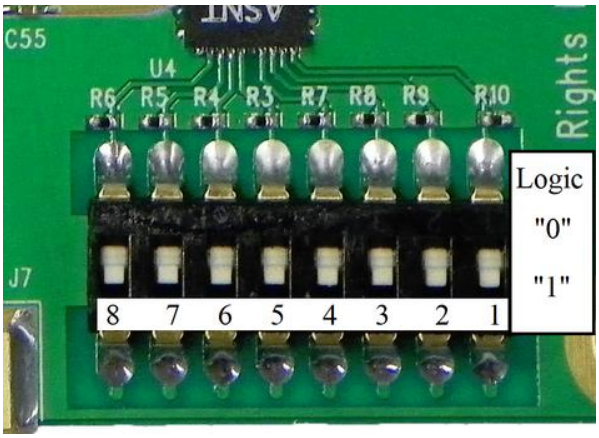

Table 1. Divide ratio

DIP SW # 8 7 6 5 4 3 2 1	n Divide Ratio	
0 0 0 0 0 0 0 1	1	
0 0 0 0 0 0 1 0	2	
0 0 0 0 0 0 1 1	3	
0 0 0 1 0 0 0 0	16	Eye diagram
. .		
0 1 1 1 1 1 1 1	127	pattern
1 1 1 1 1 1 1 0	254	pattern
0 0 0 0 0 0 0 0	256	

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		+3.6	*V*
Power Consumption		3.6	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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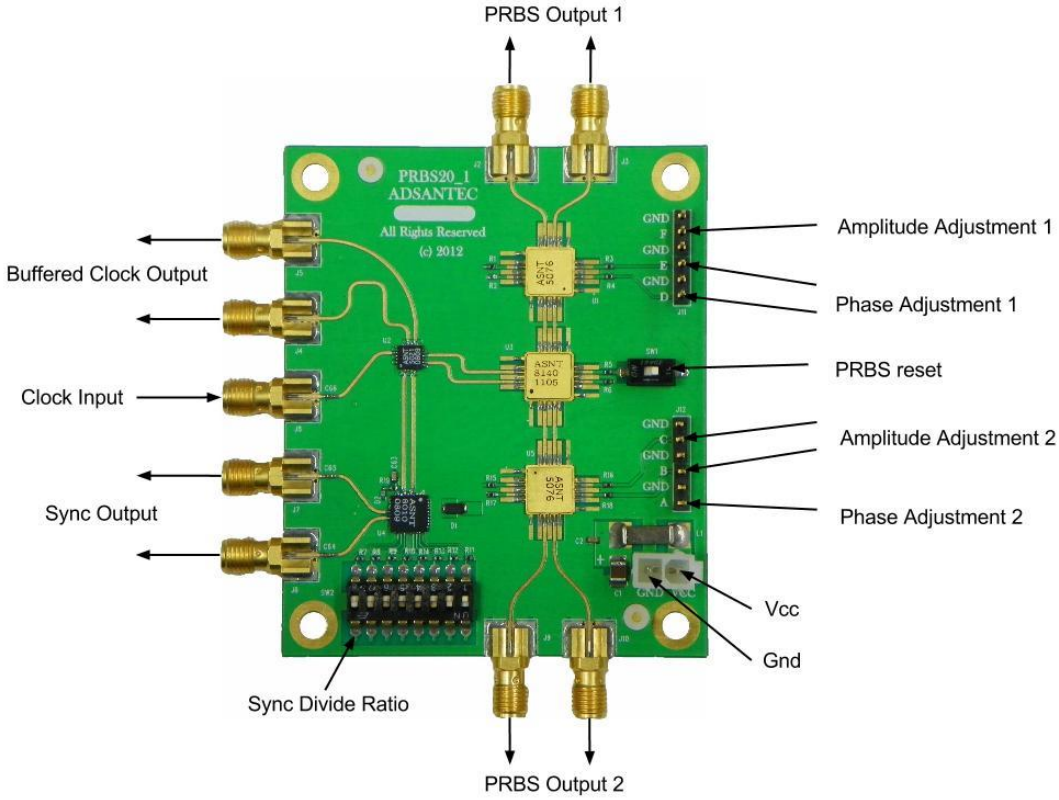
TERMINAL FUNCTIONS



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OPERATION

1. Measure 50*Ohms* on all nine SMA connectors referenced to vcc. Measure 390*Ohms* on headers A, D, and E referenced to vcc. Measure 2.2*kOhms* on headers B, C, and F referenced to vcc.
2. Connect the board to a power supply set to 0*V* with a current limit of 2*A*.
3. Slowly increase the power supply voltage to +3.3*V*. Nominal current is 1.8*A*.
4. Apply an AC coupled clock signal to the Clock Input with a frequency up to 17*GHz*, and amplitude from 50*mV* to 1*V* peak-to-peak.
5. Connect the PRBS outputs to a 50*Ohm* terminated oscilloscope. Place 50*Ohm* AC coupled terminations on all unused connections. Outputs can be used single-ended or differentially.
6. Turn PRBS reset to the ON position and then back to the OFF position to reset the PRBS generator.

   Note: Voltage values for the tuning range can be found in the electrical characteristics table for all subsequent tuning pins
7. To add jitter or change phase on the PRBS 1 output, apply a positive voltage to header pins E and D referenced to ground. These pins can be used single-ended or differentially.
8. To change the amplitude on the PRBS 1 output, apply a positive voltage to header pin F referenced to ground. The amplitude control for the PRBS 1 output is single-ended only.
9. To change the amplitude on the PRBS 2 output, apply a positive voltage to header pins B and C referenced to ground. These pins can be used single-ended or differentially.
10. To add jitter or change phase on the PRBS 2 output, apply a positive voltage to header pin A referenced to ground. This pin is single-ended only.

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}		1.8		*A*	
Power		5.9		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	0.02		18	*GHz*	
Single-Ended Swing	50	400	1000	mV_{PP}	
Clock Output					
Frequency	0.02		18	*GHz*	
Single-Ended Swing	570	600	630	mV_{PP}	
Common Mode Level	vcc -0.35	vcc -0.3	vcc -0.25		
Additive Jitter			5	*ps*	peak-to-peak
Duty Cycle	45	50	55	%	For clock signal
Sync Output					
Frequency	0.01		18	*GHz*	
Single-Ended Swing	570	600	630	mV_{PP}	
Rise/Fall Times	15	17	19	*ps*	20%-80%
Duty Cycle	45%	50%	55%		For clock signal
PRBS_1 Output					
Single-Ended Voltage Level	475	500	525	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	When Tn is NC
Duty Cycle	45	50	55	%	

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ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
PRBS_2 Output					
Single-Ended Voltage Level	475	500	525	mV_{PP}	
Common Mode Level	vcc -0.3	vcc -0.25	vcc -0.2	*V*	When Tn is NC
Duty Cycle	45%	50%	55%		
Amplitude Control					
Differential Swing	-2.85		2.85	mV_{PP}	
Common Mode Level	vcc -0.5	vcc -0.25	vcc	*V*	
Amplitude Variation	0	500	1000	*V*	
Bandwidth	0.0		100	*kHz*	
Jitter Control					
Differential Swing	-3.8		3.8	mV_{PP}	
Common Mode Level	vcc -0.5	vcc -0.25	vcc	*V*	
Phase Shift Control	0		140	*ps*	
Shift Stability	-12		12	*ps*	0-125°C
Bandwidth	0.0		500	*kHz*	

REVISION HISTORY

Revision	Date	Changes
1.3.1	05-2013	Added absolute maximum ratings Updated format
1.2.1	02-2013	Corrected low end frequency input
1.1.1	07-2012	Updated format
1.0	06-2012	Initial Release