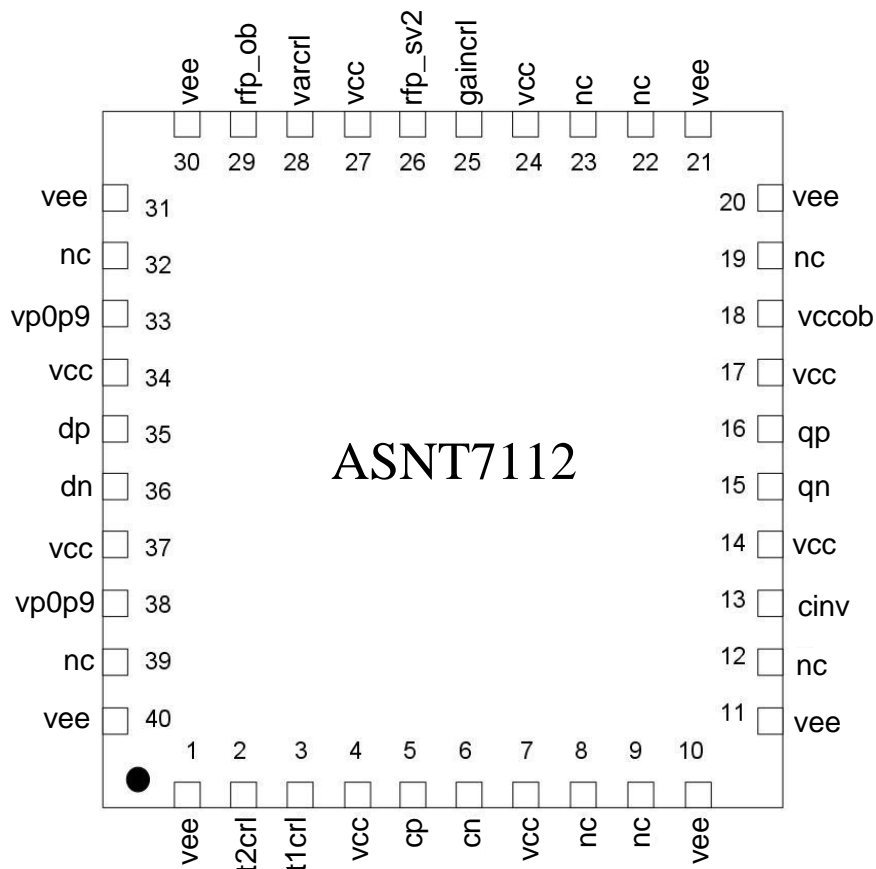




ASNT7112-PQB High-Speed Sample-and-Hold Amplifier

- More than 6-bit accuracy within the full frequency range
- Sampling speed above $2GS/s$
- Nominal $0dB$ differential gain with manual adjustment
- Adjustable duty cycle and delay of the internal sampling clocks
- Adjustable output common mode voltage level
- Adjustable input bandwidth
- Fully differential input and output data and clock buffers with on-chip 50Ω termination
- Dual $-3.2V$ and $+0.9V$ power supply
- Total power consumption of $1.75W$
- Fabricated in SiGe for high performance, yield, and reliability
- Standard 40-pin QFN package with a thermal pad





DESCRIPTION

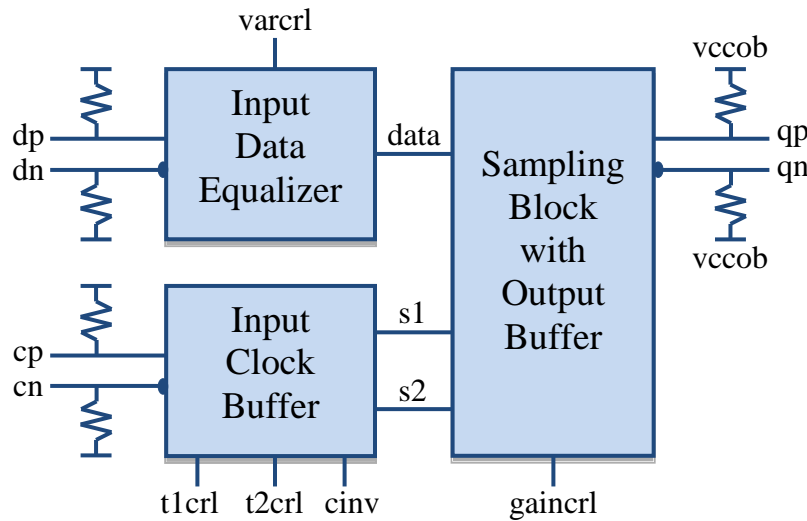


Fig. 1. Functional Block Diagram

The temperature stable and broadband ASNT7112-PQB SiGe IC is a high-speed sample-and-hold amplifier. The IC shown in Fig. 1 performs sampling of an input differential analog signal using two internally-generated strobe signals **s1** and **s2**, and delivers a step-like differential signal to the output. It features an adjustable track period length controlled by the **t1crl** and **t2crl** pins. This allows for maximizing the length of the valid output step.

The differential gain of the chip is approximately $0dB$, which corresponds to the single-ended-to-differential gain of $-6dB$. The gain is adjustable using the control pin **gaincrl**. The chip supports both AC-coupled and DC-coupled inputs. In the DC-coupled mode, the input common-mode voltage must be equal to **VCC** for optimal performance of the chip. The input sampled data path includes an equalizer that increases the bandwidth of the chip. The level of equalization is controlled with the **varcrl** pin.

The output buffer features an independent supply voltage **vccob** which allows for the adjustment of the output signal's common mode voltage. The part's outputs support the CML-type logic interface with an on-chip 50Ω termination to **VCC** and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). The differential DC signaling is recommended for optimal performance.

Input Data Equalizer

The bandwidth of the data input is controlled by the internal equalizer. The simulated frequency response of the device without the equalizer is shown in Fig. 2. The equalizer is designed to compensate for the gain drop at high frequencies. The simulated frequency response of the equalizer at different values of the **varcrl** voltage is presented in Fig. 3. Combination of the two characteristics results in a reasonably flat frequency response of the final signal device within the required bandwidth. In addition, the flatness can be controlled through the **varcrl** signal.

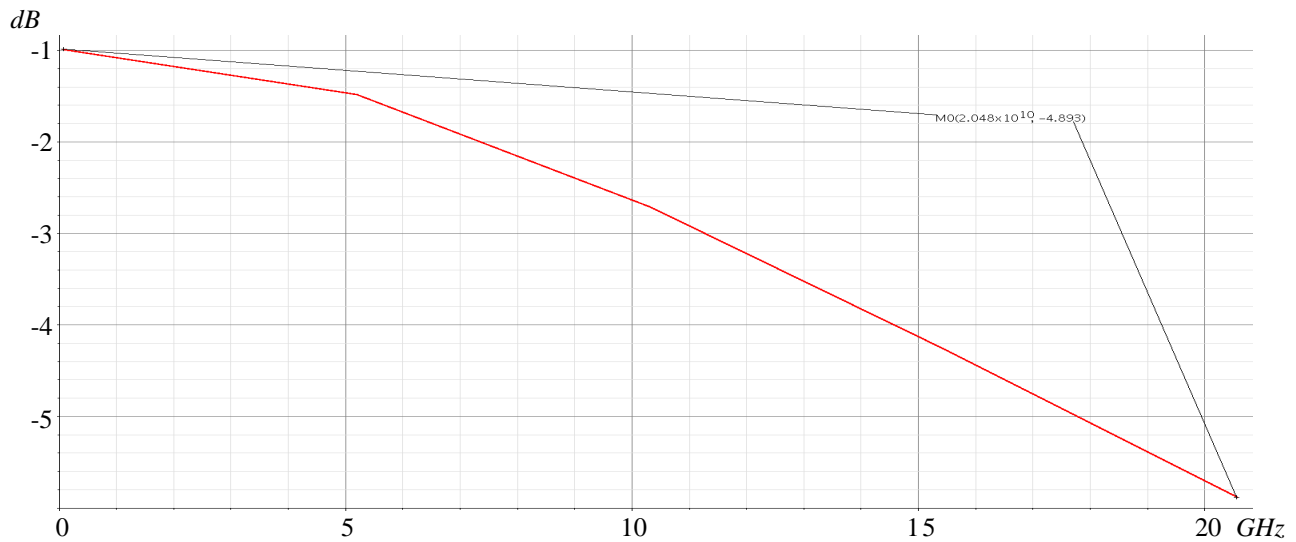


Fig. 2. Simulated Frequency Response of SHA without Equalizer

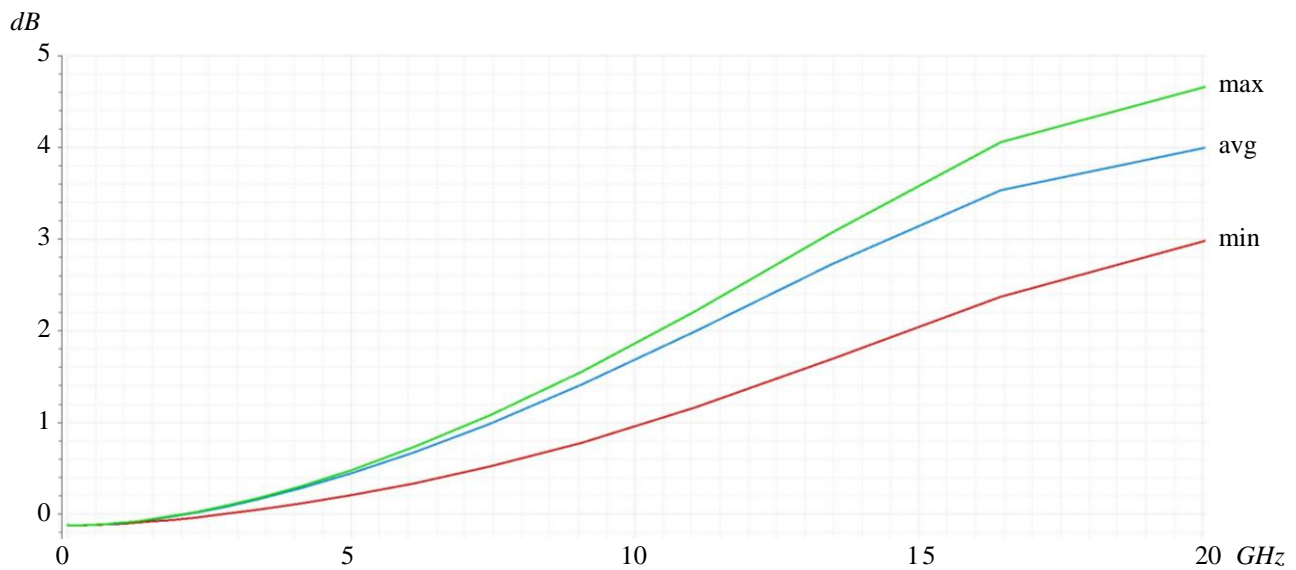


Fig. 3. Simulated Frequency Response of Equalizer at Different varcrl

Input Clock Buffer

The input clock buffer converts the external clock cp/cn into two internal signals s1 and s2 with controlled pulse width (PW) and delay (τ) between them as shown in Fig. 4.

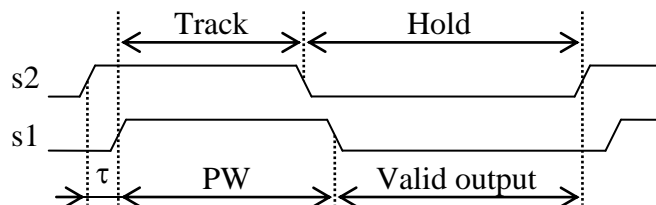


Fig. 4. Sampling Diagram



This allows for optimization of the hold time and the length of the valid output signal period. The value of PW is proportional to the t1crl voltage, while the value of τ is proportional to the t2crl voltage.

Sampling Block with Output Buffer

The sampling block performs conversion of the input signal into a step-like sampled signal under control of s1 and s2 pulses. The sampled signal is amplified by the output buffer to achieve a total gain of 0dB. The output common-mode voltage level can be directly adjusted through changing of the vccob supply voltage. The gain can be adjusted using the gaincrl voltage signal.

POWER SUPPLY CONFIGURATION

The part operates with either a negative supply scheme (vcc = 0.0V = ground, vee = -3.2V, vp0p9 = +0.9V) or a positive supply scheme (vcc = +3.2V, vee = 0V = ground, vp0p9 = +4.1V). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume the negative supply scheme.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
First Supply Voltage (vee)		-3.5	V
Second Supply Voltage (vp0p9)		+1.1	V
Power Consumption		2	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%



TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cp	5	CML input	Sampling clock inputs with internal SE 50Ohm termination to VCC
cn	6		
dp	35	Analog input	Analog sampled data inputs with internal SE 50Ohm termination to VCC
dn	36		
qp	16	CML output	Differential data outputs with internal SE 50Ohm termination to VCC. Require external SE 50Ohm termination to VCC
qn	15		
Controls			
t1crl	3	Analog voltage	Sampling clock duty cycle control.
t2crl	2	Analog voltage	Sampling clock delay control.
gaincrl	25	Analog Voltage	Gain adjustment.
varcrl	28	Analog Voltage	Equalizer peaking control.
cinv	13	CMOS Voltage	Special test pins. Leave not connected!
rfp_sv2	26	Analog Voltage	
rfp_ob	29	Analog Voltage	
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	1 st positive supply voltage (0V or 3.2V)		4, 7, 14, 17, 24, 27, 34, 37
vee	Negative power supply (-3.2V or 0V)		1, 10, 11, 20, 21, 30, 31, 40
vp0p9	Positive power supply (0.9V or 4.2V)		33, 38
vccob	Output buffer power supply		18
nc	Not connected pins		8, 9, 12, 19, 22, 23, 32, 39

Please note that pins 13, 26, and 29 should always be left not-connected! Termination of those pins may result in mal-function or damage of the part.



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.3	-3.2	-3.1	V	±3%
vcc		0		V	External ground
vp0p9	0.8	0.9	1.0		±6%
vccob	-0.3	0	0.3	V	Independent from vcc
Ivee		530		mA	
Power consumption		1750		mW	
Junction temperature	-25	50	125	°C	
Input Data (dp/dn)					
Input data frequency	0.0		14	GHz	
Swing, differential or SE, p-p	0		300	mV	THD<-50dBc from DC to max frequency
	0		400	mV	THD<-46dBc from DC to max frequency
	0		500	mV	THD<-42dBc from DC to max frequency
CM Voltage Level		vcc		V	For DC coupling
S11		-10		dB	DC to 14GHz
Input Clock (cp/cn)					
Frequency		2.0		GHz	
Swing	80		240	mV	SE or differential, p-p
CM Voltage Level	vcc-0.8		vcc-0.2	V	
Jitter			50	fs	p-p
Duty cycle	48	50	52	%	
Duty Cycle Control Voltage (t1crl)					
Voltage range	vcc – 1.1		vcc – 0.5	V	
Adjustment range		80		ps	For the pulse width of s1 and s2
Delay Control Voltage (t2crl)					
Voltage range	vcc – 1.2		vcc – 0.1	V	
Adjustment range		40		ps	For the delay of s1 vs. s2
Gain Control Voltage (gaincrl)					
Voltage range	vcc – 3.0		vcc – 0.5	V	
Equalizer Control Voltage (varcrl)					
Voltage range	vcc – 2.0		vcc	V	
Additional peaking	+3.2		+4.7	dB	At 20GHz and nominal conditions
HS Output Data (qp/qn)					
CM Level		vccob-0.4		V	
THD		TBD			
Track time range	250			ps	Length of the track period which can be increased using t1crl signal
Total DC gain	0.8		1.05		Can be adjusted using gaincrl signal
S22		-20		dB	DC to 4GHz

PACKAGE INFORMATION

The chip is packaged in a standard 40-pin QFN package shown Fig. 5. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part's identification label is ASNT7112-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

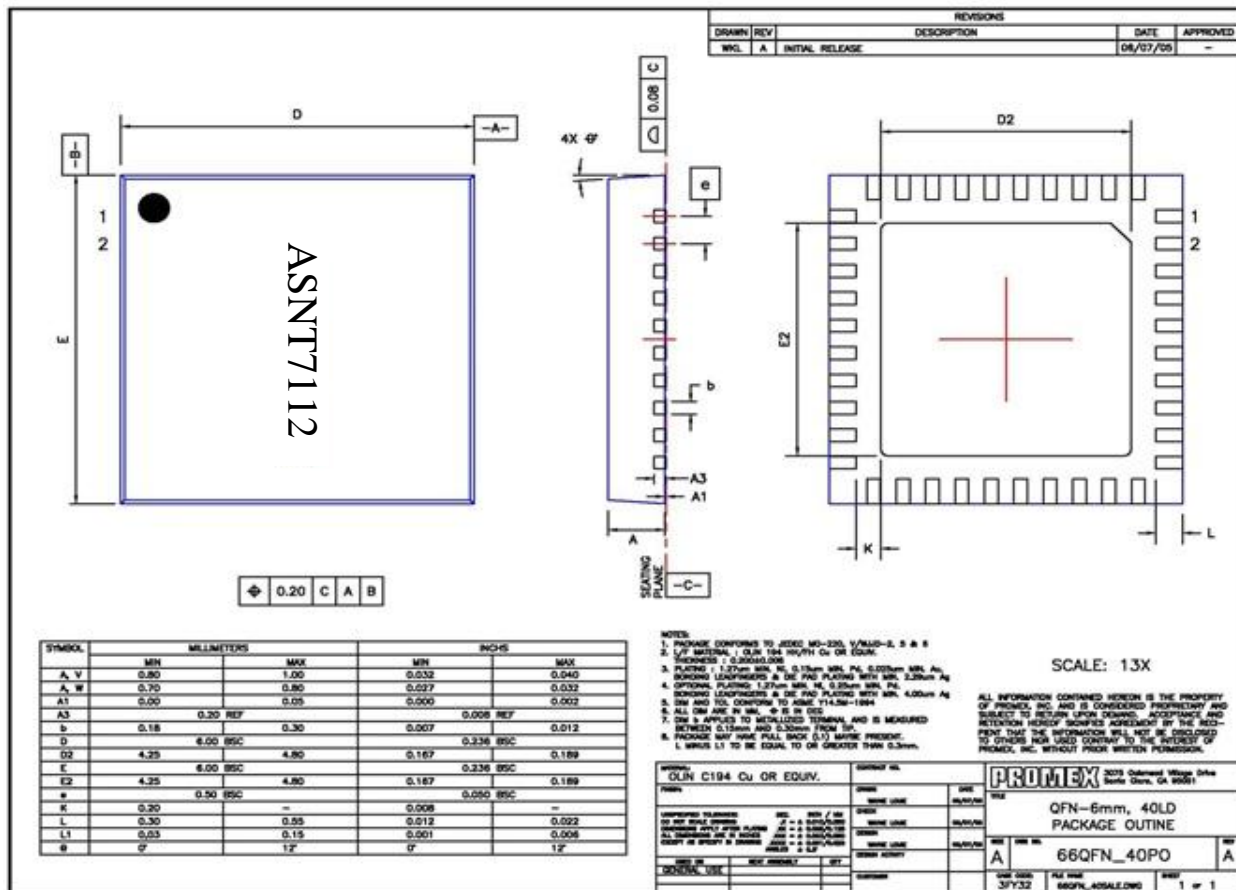


Fig. 5. QFN 40-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
1.0.1	03-2013	First release