ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
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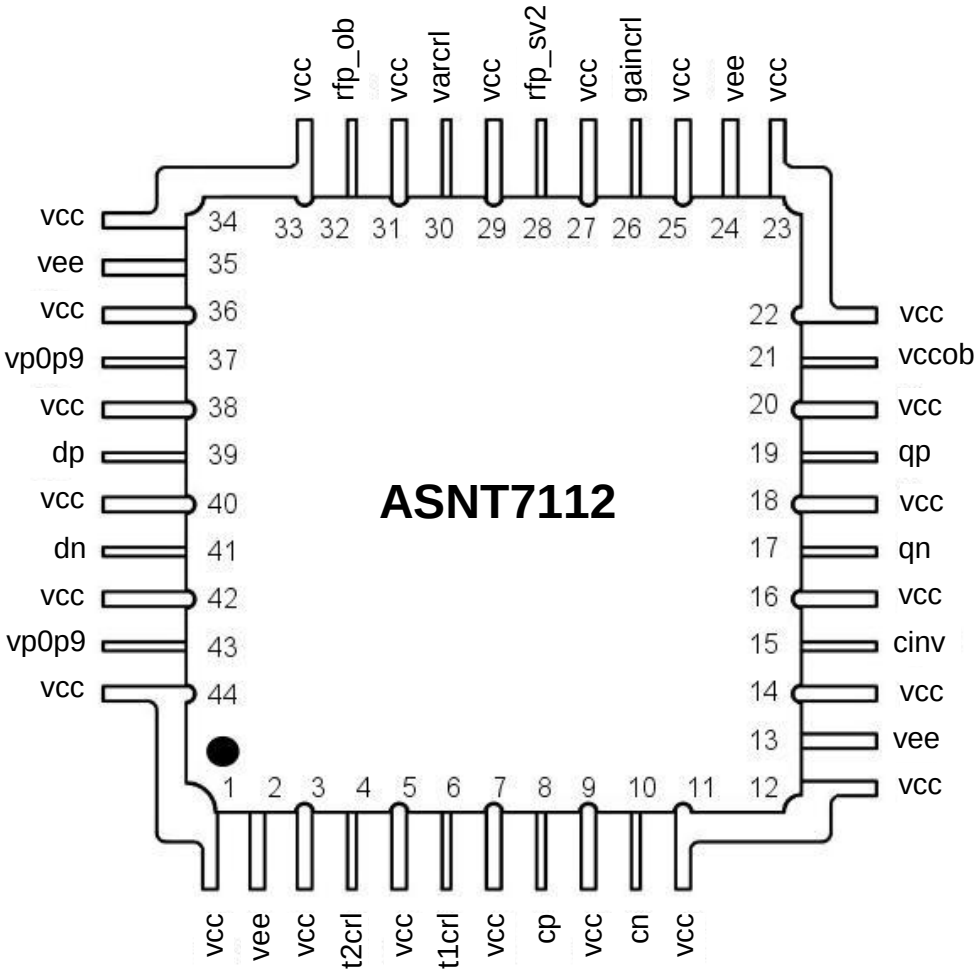
ASNT7112-KMM
High-Speed Sample-and-Hold Amplifier

- More than 6-bit accuracy within the full frequency range
- Sampling speed above 2*GS/s*
- Nominal 0*dB* differential gain with manual adjustment
- Adjustable duty cycle and delay of the internal sampling clocks
- Adjustable output common mode voltage level
- Adjustable input bandwidth
- Fully differential input and output data and clock buffers with on-chip 50*Ohm* termination
- Dual -3.2*V* and +0.9*V* power supply
- Total power consumption of 1.75*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package



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DESCRIPTION

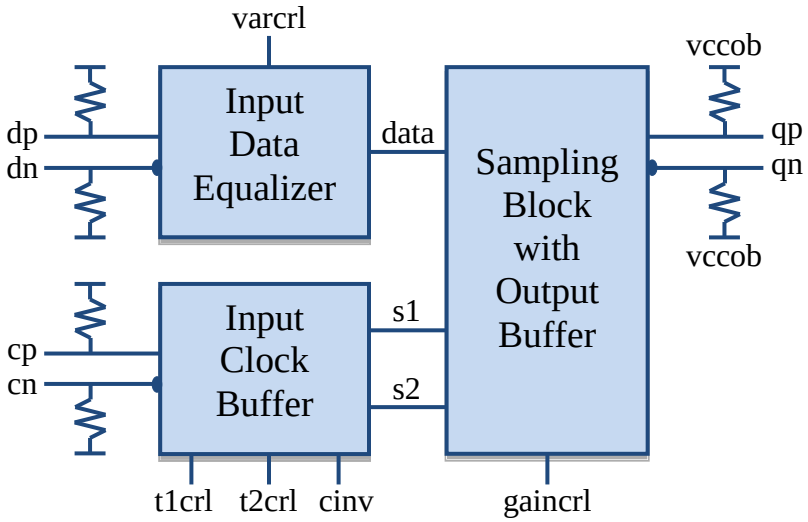

Fig. 1. Functional Block Diagram

The temperature stable and broadband ASNT7112-KMM SiGe IC is a high-speed sample-and-hold amplifier. The IC shown in Fig. 1 performs sampling of an input differential analog signal using two internally-generated strobe signals s1 and s2, and delivers a step-like differential signal to the output. It features an adjustable track period length controlled by the t1crl and t2crl pins. This allows for maximizing the length of the valid output step.

The differential gain of the chip is approximately 0*dB*, which corresponds to the single-ended-to-differential gain of -6*dB*. The gain is adjustable using the control pin gaincrl. The chip supports both AC-coupled and DC-coupled inputs. In the DC-coupled mode, the input common-mode voltage must be equal to vcc for optimal performance of the chip. The input sampled data path includes an equalizer that increases the bandwidth of the chip. The level of equalization is controlled with the varcrl pin.

The output buffer features an independent supply voltage vccob which allows for the adjustment of the output signal's common mode voltage. The part's outputs support the CML-type logic interface with an on-chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). The differential DC signaling is recommended for optimal performance.

Input Data Equalizer

The bandwidth of the data input is controlled by the internal equalizer. The simulated frequency response of the device without the equalizer is shown in Fig. 2. The equalizer is designed to compensate for the gain drop at high frequencies. The simulated frequency response of the equalizer at different values of the varcrl voltage is presented in Fig. 3. Combination of the two characteristics results in a reasonably flat frequency response of the final device within the required bandwidth. In addition, the flatness can be controlled through the varcrl signal.

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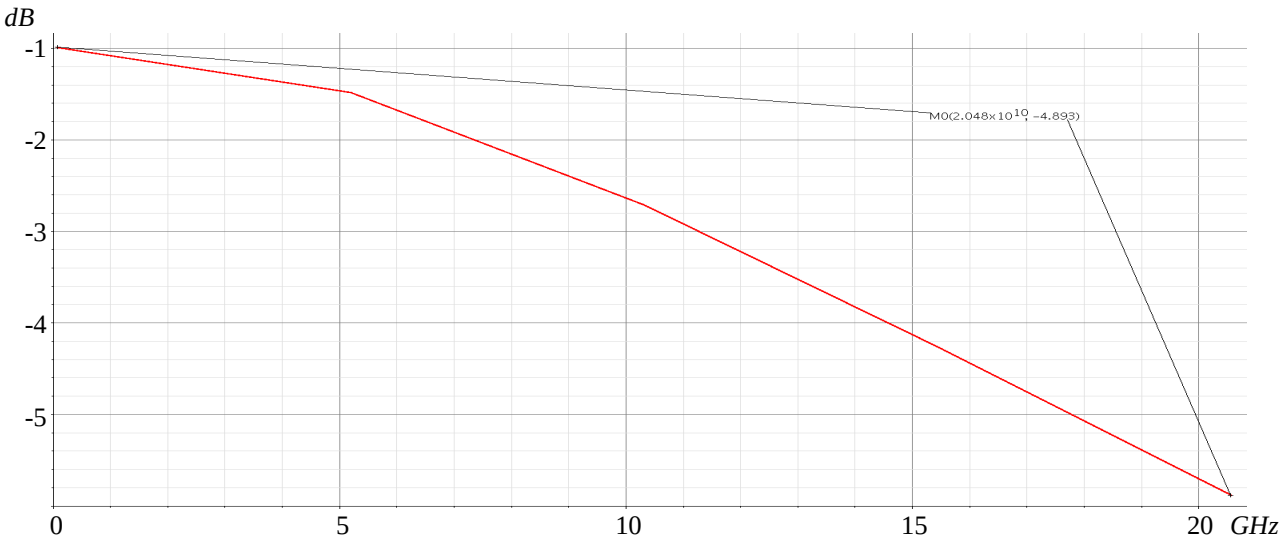

Fig. 2. Simulated Frequency Response of SHA without Equalizer

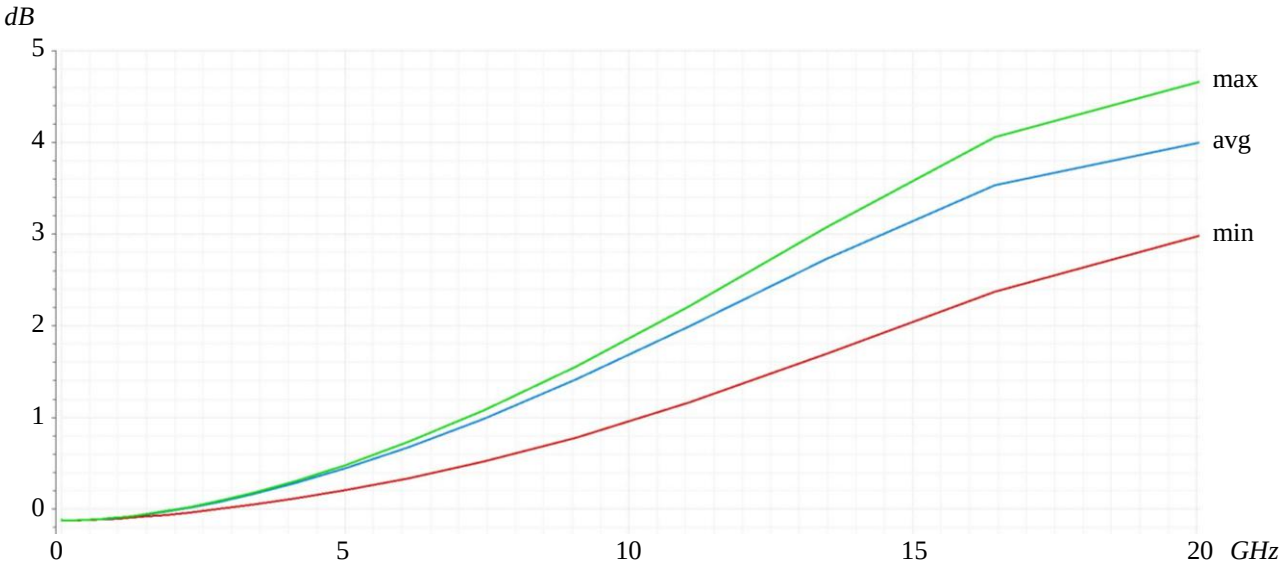

Fig. 3. Simulated Frequency Response of Equalizer at Different varcrl

Input Clock Buffer

The input clock buffer converts an external clock cp/cn into two internal signals s1 and s2 with controlled pulse width (PW) and delay (τ) between them as shown in Fig. 4.

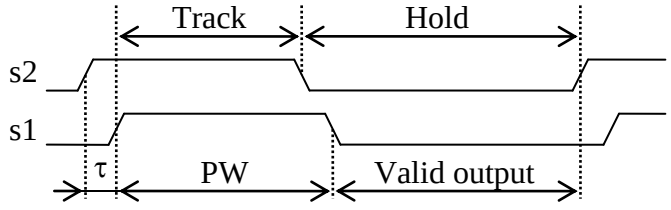

Fig. 4. Sampling Diagram

This allows for optimization of the hold time and the length of the valid output signal period. The value of PW is proportional to the t1crl voltage, while the value of τ is proportional to the t2crl voltage.

Sampling Block with Output Buffer

The sampling block performs conversion of the input signal into a step-like sampled signal under control of s1 and s2 pulses. The sampled signal is amplified by the output buffer to achieve a total gain of 0*dB*. The output common-mode voltage level can be directly adjusted through changing of the vccob supply voltage. The gain can be adjusted using the gaincrl voltage signal. The measured default frequency response of the SHA (maximum gain) is shown in Fig. 5.

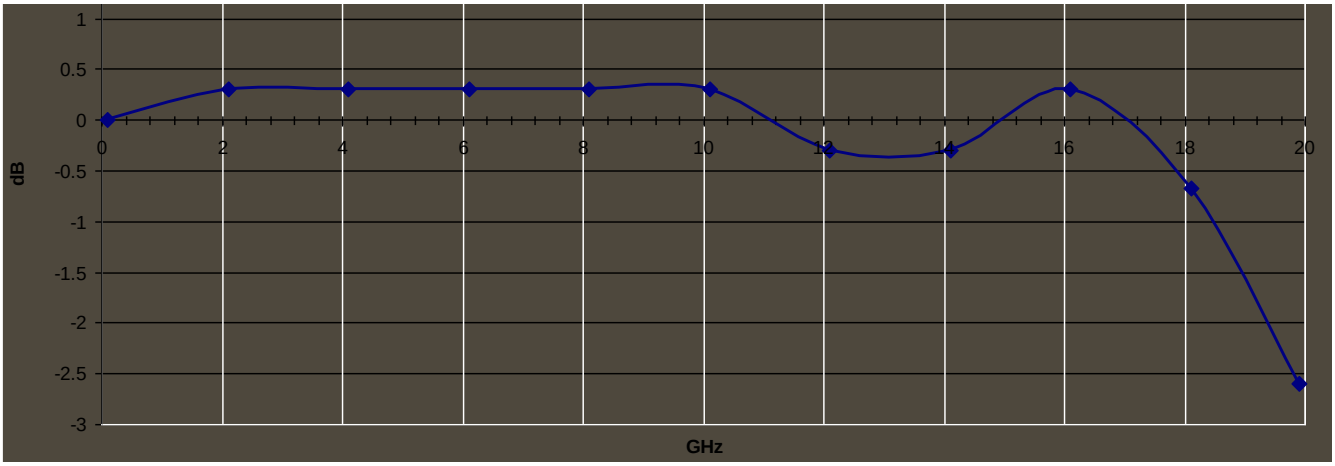

Fig. 5. SHA Gain at -6dBm Clock and -6dBm Input Data Power Levels vs. Data Frequency

The harmonic distortion of the SHA has been measured by its 3rd harmonic and is shown in Fig. 6.

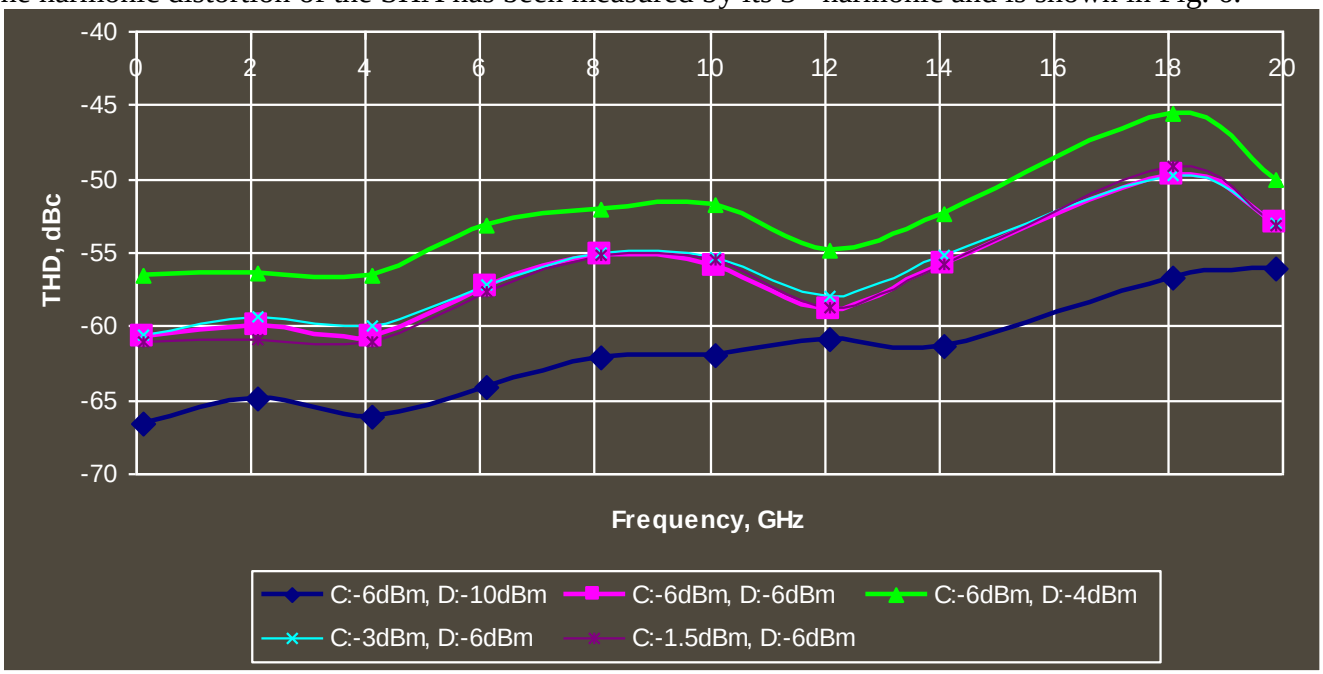

Fig. 6. Third Harmonic at Different Input Clock (C) and Data (D) Power Levels vs. Data Frequency

The part's measured noise level is shown in Fig. 7.

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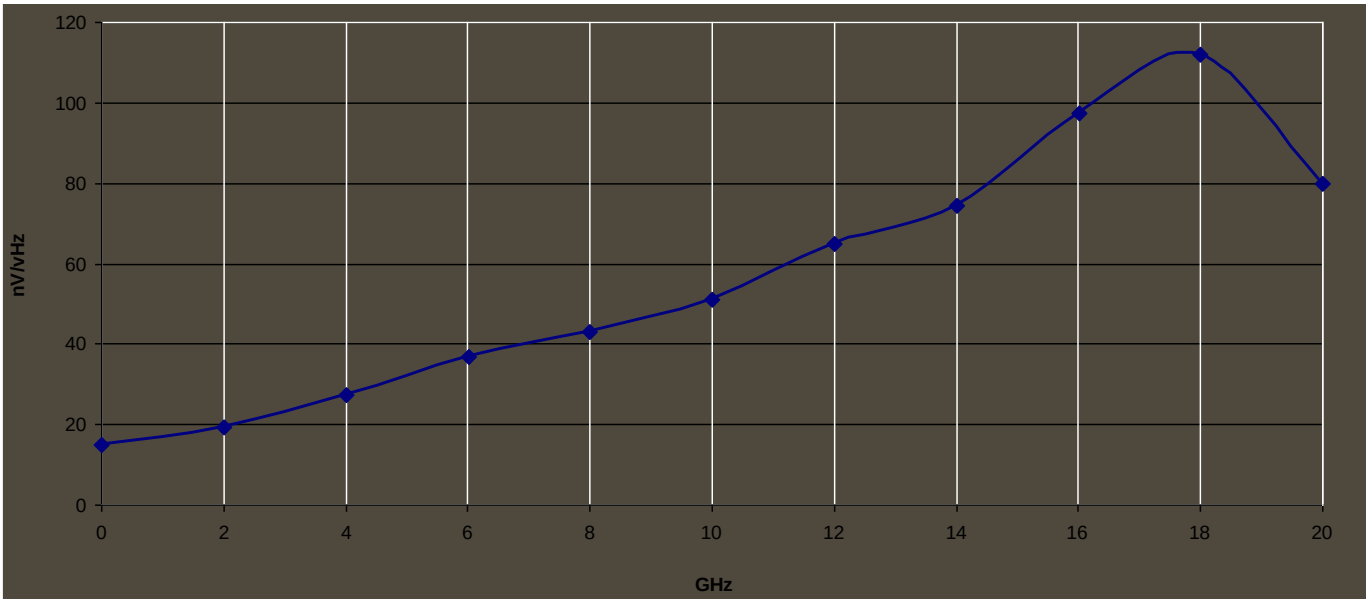

Fig. 7. Noise Figure at 2GS/s Sampling Rate vs. Input Data Frequency

POWER SUPPLY CONFIGURATION

The part operates with either a negative supply scheme (vcc = 0.0*V* = ground, vee = -3.2*V*, vp0p9 = +0.9*V*) or a positive supply scheme (vcc = +3.2*V*, vee = 0*V* = ground, vp0p9 = +4.1*V*). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume the negative supply scheme.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
First Supply Voltage (vee)		-3.5	*V*
Second Supply Voltage (vp0p9)		+1.1	*V*
Power Consumption		2	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cp	8	CML input	Sampling clock inputs with internal SE 50*Ohm* termination to VCC
cn	10		
dp	39	Analog input	Analog sampled data inputs with internal SE 50*Ohm* termination to VCC
dn	41		
qp	19	CML output	Differential data outputs with internal SE 50*Ohm* termination to VCC. Require external SE 50*Ohm* termination to VCC
qn	17		
Controls			
t1crl	6	Analog voltage	Sampling clock duty cycle control
t2crl	4	Analog voltage	Sampling clock delay control
gaincrl	26	Analog Voltage	Gain adjustment
varcrl	30	Analog Voltage	Equalizer peaking control
cinv	15	CMOS Voltage	Special test pins. **Leave not connected!**
rfp_sv2	28	Analog Voltage	
rfp_ob	32	Analog Voltage	

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	1st positive supply voltage (0*V* or 3.2*V*)	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply (-3.2*V* or 0*V*)	2, 13, 24, 35
vp0p9	Positive power supply (0.9*V* or 4.2*V*)	37, 43
vccob	Output buffer power supply	21

Please note that pins 15, 28, and 32 should always be left not-connected! Termination of those pins may result in mal-function or damage of the part.

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.3	-3.2	-3.1	*V*	±3%
vcc		0		*V*	External ground
vp0p9	0.8	0.9	1.0		±6%
vccob	-0.3	0	0.3	*V*	Independent from vcc
*I*vee		530		*mA*	
Power consumption		1750		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Data (dp/dn)					
Input data frequency	0.0		20	*GHz*	
Swing, differential or SE, p-p	0		300	*mV*	THD<-50*dBc* from DC to max frequency
	0		400	*mV*	THD<-46*dBc* from DC to max frequency
	0		500	*mV*	THD<-42*dBc* from DC to max frequency
CM Voltage Level		vcc		*V*	For DC coupling
S11		-10		*dB*	DC to 20*GHz*
Input Clock (cp/cn)					
Frequency		2.0		*GHz*	
Swing	80		240	*mV*	SE or differential, p-p
CM Voltage Level	vcc-0.8		vcc-0.2	*V*	
Jitter			50	*fs*	p-p
Duty cycle	48	50	52	*%*	
Duty Cycle Control Voltage (t1crl)					
Voltage range	vcc – 1.1		vcc – 0.5	*V*	
Adjustment range		80		*ps*	For the pulse width of s1 and s2
Delay Control Voltage (t2crl)					
Voltage range	vcc – 1.2		vcc – 0.1	*V*	
Adjustment range		40		*ps*	For the delay of s1 vs. s2
Gain Control Voltage (gaincrl)					
Voltage range	vcc – 3.0		vcc – 0.5	*V*	
Equalizer Control Voltage (varcrl)					
Voltage range	vcc – 2.0		vcc	*V*	
Additional peaking	+3.2		+4.7	*dB*	At 20*GHz* and nominal conditions
HS Output Data (qp/qn)					
CM Level		vccob-0.4		*V*	
THD					See Fig. 6
Track time range	250			*ps*	Length of the track period which can be increased using t1crl signal
Total DC gain	0.8		1.05		Can be adjusted using gaincrl signal
S22		-20		*dB*	DC to 4*GHz*

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PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 8. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the VCC plain that is ground for the negative supply or power for the positive supply.

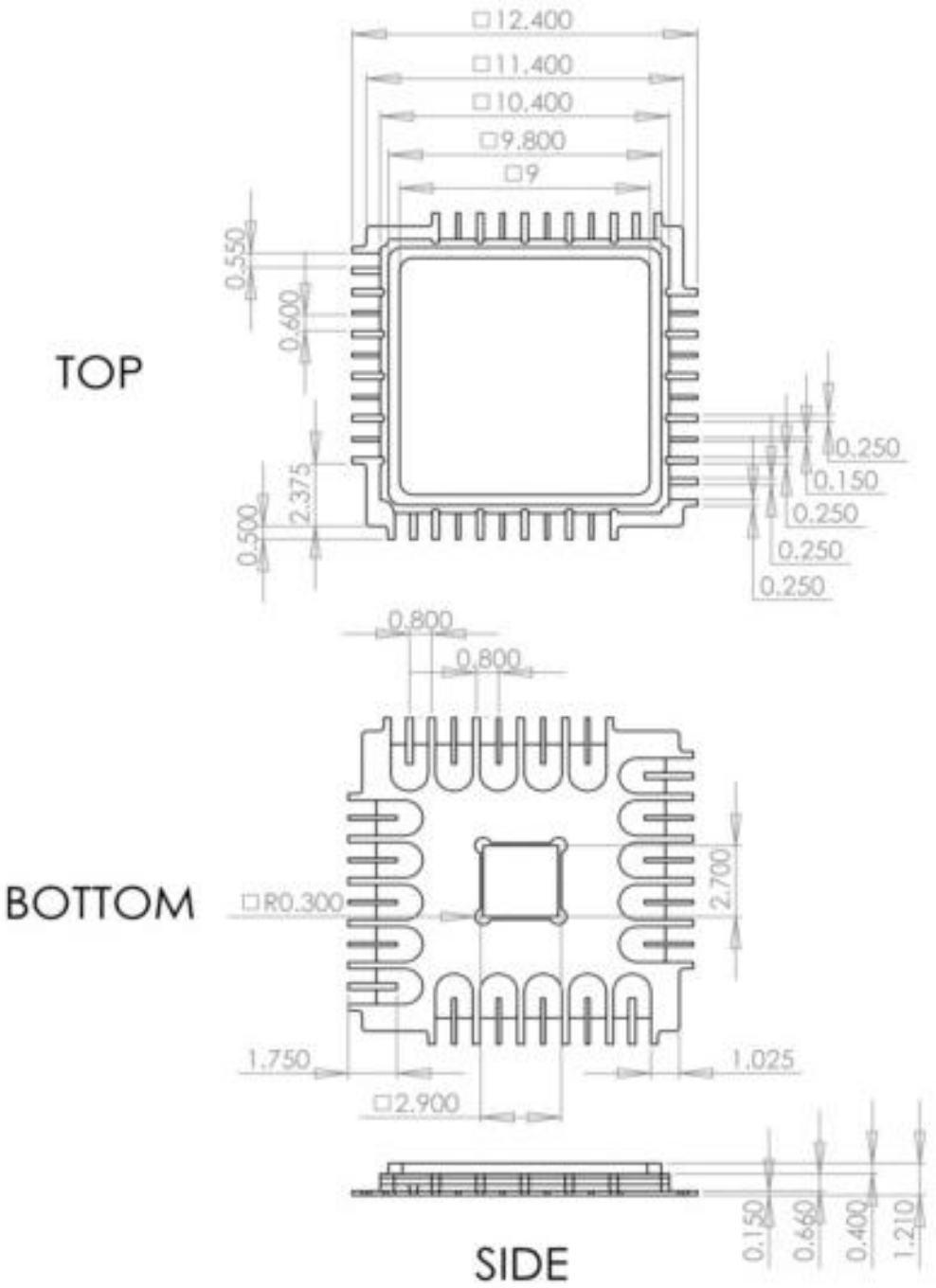

Fig. 8. CQFP 44-Pin Package Drawing (All Dimensions in mm)

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The part's identification label is ASNT7112-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.2.1	03-2013	Corrected electrical characteristics
1.1.1	02-2013	Corrected description Added simulation and measured data Corrected electrical specifications
1.0.1	08-2012	First release