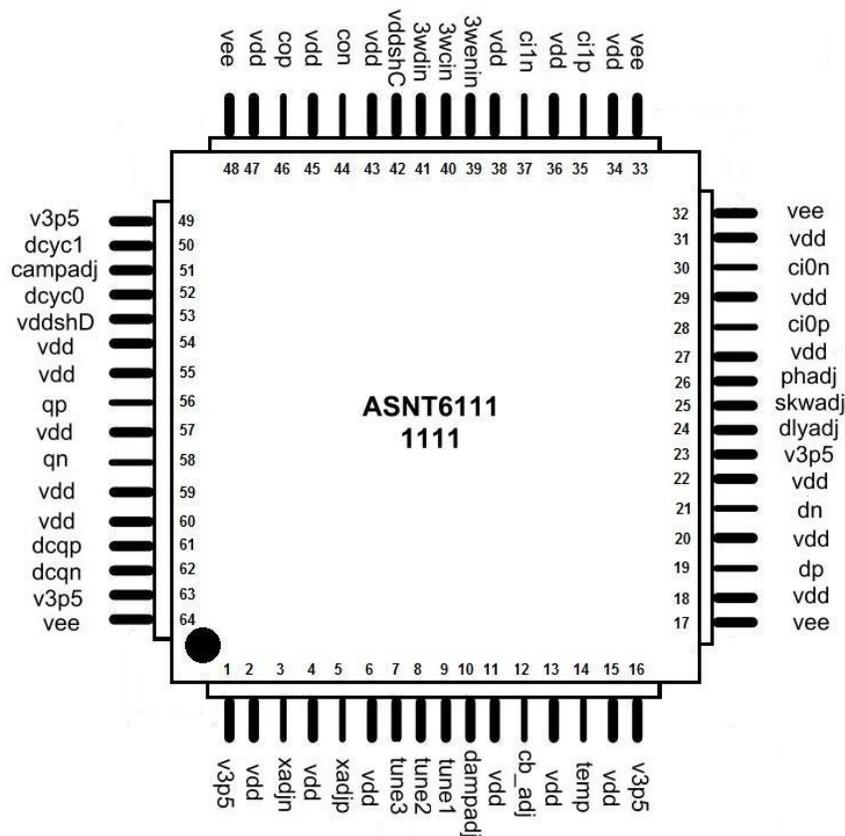




ASNT6111-KMF 30Gbps Advanced Driver/Amplifier

- High-speed limiting amplifier with selectable built-in pre-emphasis.
- Four pre-emphasis taps with externally controlled weight and inversion.
- Adjustable data output amplitude and eye quality.
- Single-ended output data eye cross point adjustment.
- Optional main clock frequency multiplier by 2.
- Duty cycle indicators for the main clock before and after the multiplier.
- Opposite and parallel adjustment of the main clock and data delays.
- Additional clock input.
- Fully differential CML input and output data and clock interfaces.
- Selectable main or additional clock at the output with adjustable amplitude.
- CMOS 3-wire interface for digital controls.
- On-chip linear temperature sensor.
- Two power supplies: negative -4.3V and floating positive +3.5V.
- Power consumption: <4.4W.
- Custom CQFP 64-pin package.





DESCRIPTION

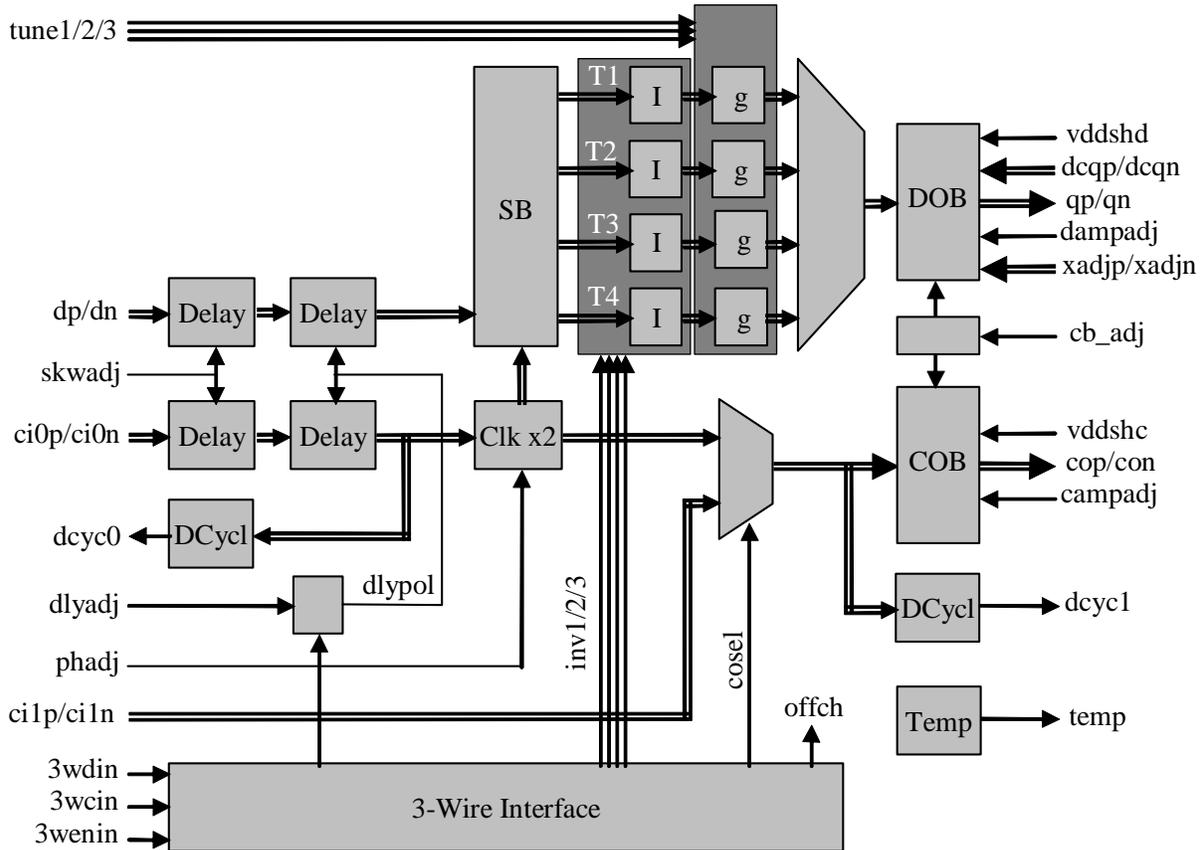


Fig. 1. Functional Block Diagram

The ASNT6111-KMC SiGe IC shown in Fig. 1 is an advanced programmable driver amplifier (ADA) with built-in 4-tap pre-emphasis. ADA generates a combination of four delayed copies of its input differential data signal *dp/dn* with certain user-controlled weights and polarities. The copies are created in a 4-bit shift register activated by internal high-speed clock signal (see Sampling Block and Taps). This clock signal is a copy of the main input clock *ci0p/ci0n* with either matching or doubled frequency. In the multiply-by-2 clock mode, the duty cycles of the input and internal clock signals are monitored and the output duty cycle can be adjusted through external control port *phadj* (see Clock Multiplier).

Input clock and data signals can be delayed in the same or opposite directions to ensure their correct phase relations at the inputs of the shift register and at the chip outputs (see Input Delay Section). ADA can accept one additional clock signal *ci1p/ci1n* and deliver it to output *cop/con* instead of the main clock “*ci0p/n*”, thus operating as a clock buffer (see Additional Input Clock and Clock Output Buffer).

The part’s I/Os support CML logic interface with on-chip *50Ohm* termination to ground. External *50Ohm* termination is required. DC-coupling for data and clock output ports is strongly recommended. The input ports can use DC or AC coupling. Amplitude and peaking in the clock and data output signals can be externally adjusted. Both single-ended data output signals also have controlled DC common-mode levels and eye crossing points (see Data Output Buffer).



The operational modes of the chip are controlled through a 3-wire serial interface (see 3-Wire Interface Control Block).

The chip operates from one negative power supply (positive pin connected to external Ground, negative pin $v_{ee} = -4.3V$) and one floating positive power supply (negative pin connected to v_{ee} and positive pin $v_{3p5} = 3.5V$). It is recommended to keep the relative deviation of v_{3p5} from Ground within less than $\pm 0.1V$.

Input Delay Section

As shown in Fig. 1, ADA accepts differential input data dp/dn and clock $ci0p/ci0n$ signals and inserts them both into identical variable delay blocks **Delay** that can be oppositely adjusted by external analog control voltage $skwadj$ in order to eliminate skew between the two channels. The blocks can compensate the skew up to $\pm 15ps$. Subsequently, both input signals are further processed by two additional **Delay** blocks that can be adjusted in parallel or opposite modes depending on the polarity of internal digital signal $dlypol$ (“0”=parallel, “1”=opposite) provided by the 3-Wire Interface block. This second pair of **Delay** blocks allows for external adjustment of the data vs. clock signals when operating in opposite mode or varying the delay of the output data and clock signals when in parallel mode. The delay adjustment range is $\pm 75ps$ in the opposite mode or $0-75ps$ in the parallel mode.

Clock Multiplier

The clock doubler $Clkx2$ uses a “delay and XOR” mechanism to create output clock pulses from each edge of the input clock $ci0p/ci0n$. The multiplier is intended for operation with input clock signals within the frequency range from $4GHz$ to $15GHz$. Analog control voltage $phadj$ performs a dual function. Voltages within the range from $0V$ to $-2.0V$ activate the multiplication function and are used for tuning the block’s internal delay in order to achieve 50% duty cycle of the multiplied clock. Voltages between $-2.0V$ and v_{ee} disable the multiplication function and allow for direct passing of the input clock to the multiplier’s output. This mode should be used for operation with clock signal frequencies below $14GHz$.

Two duty cycle control blocks $DCycl$ are used for monitoring the clock pulse shapes before and after the multiplier. The first block is positioned before the multiplier and delivers single-ended analog voltage $dcyc0$ that indicates the input clock’s duty cycle deviation from 50%. The second block is positioned after the multiplier and delivers similar signal $dcyc1$ for the output clock. Both generated output voltages can be used in combination with $phadj$ input within external control loops for getting an optimal shape of the multiplied clock.

Additional Input Clock and Clock Output Buffer

ADA can also accept an additional input clock signal $ci1p/ci1n$ and deliver it to the clock output. This allows the IC to operate solely as a clock amplifier where the output clock signal’s amplitude supplied by output buffer **COB** can be adjusted using analog signal $campadj$. The amplitude range is from $0V_{pp}$ ($campadj \leq -2.0V$) to $900mV_{pp}$ ($campadj = 0V$) single ended. **COB** can also be completely disabled by applying $campadj$ voltage between $-2.0V$ and v_{ee} . Either $ci0$ or $ci1$ clock signal can be processed by output buffer **COB**. Selection of the input clock is accomplished through digital control signal **clock select** (“0” - $ci0$, “1” - $ci1$) delivered by the 3-wire interface block.



Quality of the output signal shape can be optimized using control voltages **cb_adj** and **vddshc**. The first voltage controls the default position of the output eye crossing point and peaking on the rising edge of the output signal (weak influence). The allowed voltage range is from 0V to **vee**. The second (positive) voltage controls peaking on the falling edge of the output signal (strong influence). The allowed voltage range is from 2.8V to 4.3V with the negative pin of the supply connected to **vee**. In both cases, more positive voltages correspond to more peaking.

Sampling Block and Taps

Sampling block **SB** is essentially a 4-bit shift register that generates 4 delayed bits **T1-T4** needed for ADA's 4-tap pre-emphasis capability. As stated above, analog control voltage **dlyadj** is used to adjust the phase relationship between clock and data to ensure optimum sampling in **SB**. All four samples delivered by **SB** can be independently inverted by circuit blocks **I**, where the polarity of the signals is set by four control signals **inv0/inv1/inv2/inv3** ("0"=direct, "1"=inverted) provided by the 3-wire interface.

The weights of taps are set by the gain adjustment blocks **g** that are controlled by a special current distributing circuitry using three external analog voltages **tune1/tune2/tune3**. The circuitry operates in such a way that the first control voltage **tune1** either defines the fraction of the main current that is used in the first tap (0V corresponds to full current and -2.0V corresponds to no current), or disables the first tap completely (voltages below -2.0V). The remaining current is distributed between the second and the third taps in the same way in accordance with the value of the second control voltage **tune2**, and then between the third and the fourth taps in accordance with the value of the third control voltage **tune3**. Thus, the total current (and weight) is independent from the number of activated taps and their individual settings. High value (~0V) of a certain **tuneX** signals can be used for disabling all subsequent taps based on internal thresholds. This function can be activated/deactivated through digital control signal **offch** ("0" – thresholds activated, "1" – thresholds deactivated) delivered by the 3-wire interface block. The combined current from the taps is delivered to data output buffer **DOB** for the final signal conditioning.

Data Output Buffer

Data output buffer **DOB** includes several features to tune the output data signal generated by ADA. Similar to **COB**, adjustment of the output data's amplitude is possible by means of external analog control voltage **dampadj**. The amplitude range is from 0.0V_{pp} (**dampadj**≤-2.0V) to 1.3V_{pp} (**dampadj**=0V) single-ended.

Differential analog control voltage **xadjp/xadjn** can be utilized to adjust the crossing points in the single-ended output eyes. At the default state of **xadjp=xadjn=0V**, the crossing points in both direct and inverted eyes should be centered. The crossing points are moving up in the direct eye and down in the inverted eye if **xadjp=-xadjn**>0, or in the opposite directions if **xadjp=-xadjn**<0. The allowed voltage range of ±4.0V corresponds to shifts of the crossing points up to ±25% of the eye amplitude.

Quality of the output signal shape can be optimized using control voltages **cb_adj** and **vddshd** as described in Clock Output Buffer section above.



Finally, 1.0KOhm resistors are attached to both data outputs qp and qn to provide DC shifting of the output signals. Access to the resistors is through the control pins dcqp/dcqn. The allowable DC voltage that can be applied to those pins is from 0 to vee.

3-Wire Interface Control Block

To reduce the physical number of digital control inputs to ADA, an 8-bit shift register with a 3-wire input interface has been included on chip. The digital control bits applied through 3wdin input are latched in and shifted down the register by negative edges of low-speed clock 3wcin. Write enable signal 3wenin must be set to logic “1” during the data read-in phase and then set to logic “0” to retain the shifted in values after 8 clock periods of 3wcin. All input signals should have voltage levels of $V^{H1}=0V$ and $V^{H0}=-3.3V$. The maximum frequency of 3wcin clock is 100KHz. Table 1 below maps the input 8-bit word to the internal digital control signals.

Table 1. 3-Wire Interface Bit Map.

Input Digital Data Byte 3wdin	Internal Digital Control Signal
8 th Bit (last serial bit)	tap1 inversion (“0”=direct, “1”=inverted)
7 th Bit	tap2 inversion (“0”=direct, “1”=inverted)
6 th Bit	tap3 inversion (“0”=direct, “1”=inverted)
5 th Bit	tap4 inversion (“0”=direct, “1”=inverted)
4 th Bit	dlyadj polarity (“0”=parallel, “1”=opposite)
3 rd Bit	output clock select (“0”=ci0, “1”=ci1)
2 nd Bit	tap thresholds (“0”=enabled, “1”=disabled)
1 st Bit (first serial bit)	Not used

Temperature Sensor

A linear temperature sensor is included on chip. Its behavior is illustrated in Fig. 2 below.

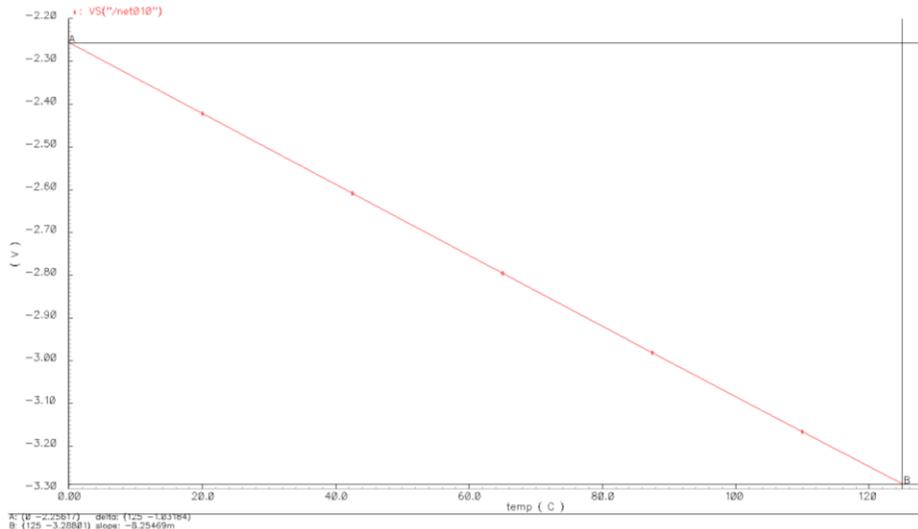


Fig. 2. Temperature Sensor’s Characteristic.



TERMINAL FUNCTIONS

TERMINAL			Description	
Name	No.	Type		
<u>High-Speed I/Os</u>				
dp	19	CML Inputs	Differential high-speed data inputs	
dn	21			
ci0p	28		Differential high-speed main clock inputs	
ci0n	30			
ci1p	35			Differential high-speed additional clock inputs
ci1n	37			
cop	46	CML Outputs	Differential high-speed clock outputs	
con	44			
qp	56		Differential high-speed data outputs	
qn	58			
<u>Low-Speed I/Os</u>				
3wenin	39	3.3V	Enable input signal for 3-wire interface	
3wcin	40	CMOS Inputs	Clock input signal for 3-wire interface	
3wdin	41		Data input signal for 3-wire interface	
<u>Analog Control Voltage Inputs</u>				
xadjp	5	Analog Inputs with 100KOhm termination to vdd.	Output data eye cross point adjustment, Differential	
xadjn	3			
tune3	7		Tap 3 weight adjustment, SE	
tune2	8		Tap 2 weight adjustment, SE	
tune1	9		Tap 1 weight adjustment, SE	
dampadj	10		Data output amplitude adjustment, SE	
cb_adj	12		Cascode bias current adjustment, SE	
dlyadj	24		Data/clock skew/output phase adjustment, SE	
skwadj	25		Data/clock skew adjustment, SE	
phadj	26		Clock multiplier delay (output duty cycle) adjustment, SE	
campadj	51		Clock output amplitude adjustment, SE	
dcqp	61		Analog Inputs	Direct data output common-mode DC shift, SE
dcqn	62			Inverted data output common-mode DC shift, SE
<u>Analog Control Indicators</u>				
temp	14	Analog Outputs	Linear temperature-dependent voltage	
dcyc1	50		Linear voltage indicating output clock duty cycle	
dcyc0	52		Linear voltage indicating main input clock duty cycle	



Supply And Termination Voltages

Name	Description	Pin Number
vdd	External ground	2,4,6,11,13,15,18,20,22,27,29,31,34,36,38,43,45,47,54,55,57,59,60
vee	-4.3V negative power supply	17,32,33,48,64
v3p5	+3.5V positive power supply. Negative pin to vee	1,16,23,49,63
vddshC	Output clock and data peaking adjustment.	42
vddshD	Positive power supply. Negative pin to vee	53

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed VCC).

Table 2. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Negative Supply Voltage (vee)		-4.8	V
Positive Supply Voltage (v3p5)		3.8	V
Power Consumption		4.8	W
RF Input Voltage Swing (SE)		1.2	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-4.1	-4.3	-4.5	V	
vcc		0.0		V	External ground
v3p5	3.4	3.5	3.6	V	“-“ pin to vee
Ivcc		180		mA	
Iv3p5		1000		mA	
Power		4.3		W	
Allowed junction temperature	0	50	100	°C	
Data input (dp/dn)					
Rate	DC		30	Gb/s	
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vcc-(SE swing)/2				
Clock input (ci0p/ci0n, ci1p /ci1n)					
Frequency	0.1		18	GHz	
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vcc-(SE swing)/2				
Data output (qp/qn)					
Rate	DC		30	Gbps	
SE Swing	0.0		1300	mV	Peak-to-peak
CM Level	vcc		vcc-0.65	V	
Rise/Fall Times	10	12	14	ps	20%-80%
Clock output (cop/con)					
SE Swing, max	600		900	mV	Pk-pk, 0-15GHz
SE Swing, max	200		650	mV	Pk-pk, 15-25GHz
SE Swing, max	150		220	mV	Pk-pk, 25-28GHz
CM Level	vcc		vcc-0.4	V	
Rise/Fall Times	10	12	14	ps	20%-80%
SE tuning ports (tune1/2/3, skwadj dlyadj phadj dampadj campadj)					
Linear control voltage	-2		0	V	
Switch-off threshold		-2		V	
Cross point control (xadjp/xadjn)					
Differential voltage range	-8.0		8.0	V	±4V at each input
CM Level	vcc				
Current into the pin		4		mA	at +4V
Current out of the pin		-4		mA	at -4V
Bias control (cb adj)					
Voltage range	vee		vcc	V	
DC common mode voltage control (dcqp/dcqn)					
Voltage range	vee		vcc	V	



PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Variable supply voltages (vddshc, vddshd)					
Voltage range	2.8		4.3	V	“-“ pin to vee
I_{vddshd}		18		mA	All 4 taps active.
I_{vddshc}		1.1		mA	
Duty Cycle Indicator (dcyc0/1)					
Voltage range	-3.3		-0.8	V	
Temperature Sensor (temp)					
Voltage range	-3.3		-2.3	V	
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	-0.2		0.0	V	
Low voltage level	-3.3		-3.1	V	
Clock speed			100	KHz	

PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 3. The package’s mechanical information is also available on the company’s [website](#). The package’s leads will be trimmed to a length of 1.0mm. After trimming, the package’s leads will be further processed as follows:

1. The lead’s gold plating will be removed per the following sections of J-STD-001D:
 - 3.9.1 Solderability
 - 3.2.2 Solder Purity Maintenance
 - 3.9.2 Solderability Maintenance
 - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder.

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to “vcc” plain that is ground for the negative supply or power for the positive supply.

The part’s identification label is ASNT6111-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.



64-PIN KMF Package

All Dimensions are in millimeters

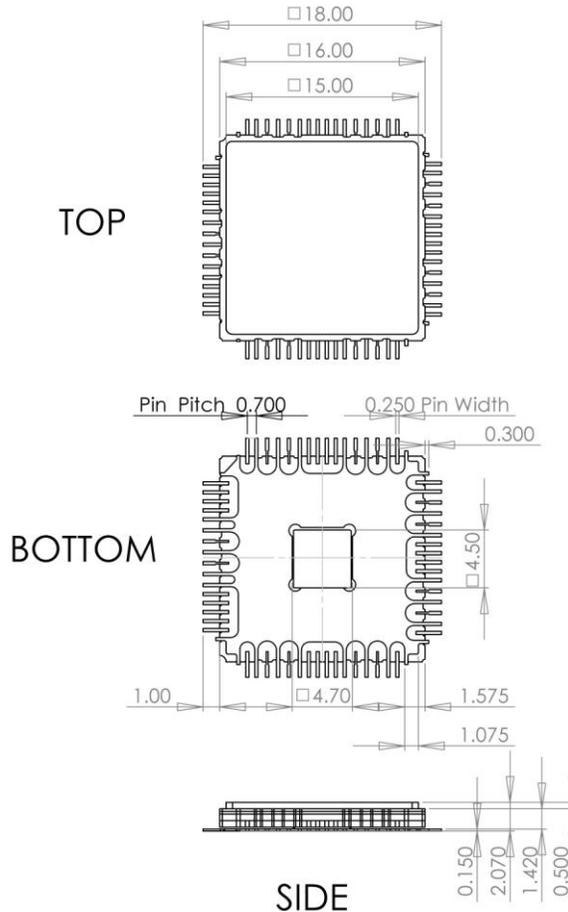


Fig. 3. Package Drawing.

REVISION HISTORY

Revision	Date	Changes
3.5.1	10-2012	Corrected control voltage range for vddshC and vddshD
3.4.1	10-2012	Corrected description. Corrected electrical characteristics.
3.3.1	08-2012	Corrected format.
3.3	05-2012	Corrected description. Corrected Electrical Parameters (based on measurements).
3.2	04-2012	Added Pin Diagram. Added Absolute Maximums Rating table. Revised Package Information section. Added Revision History table.
3.1	12-2011	First release.