ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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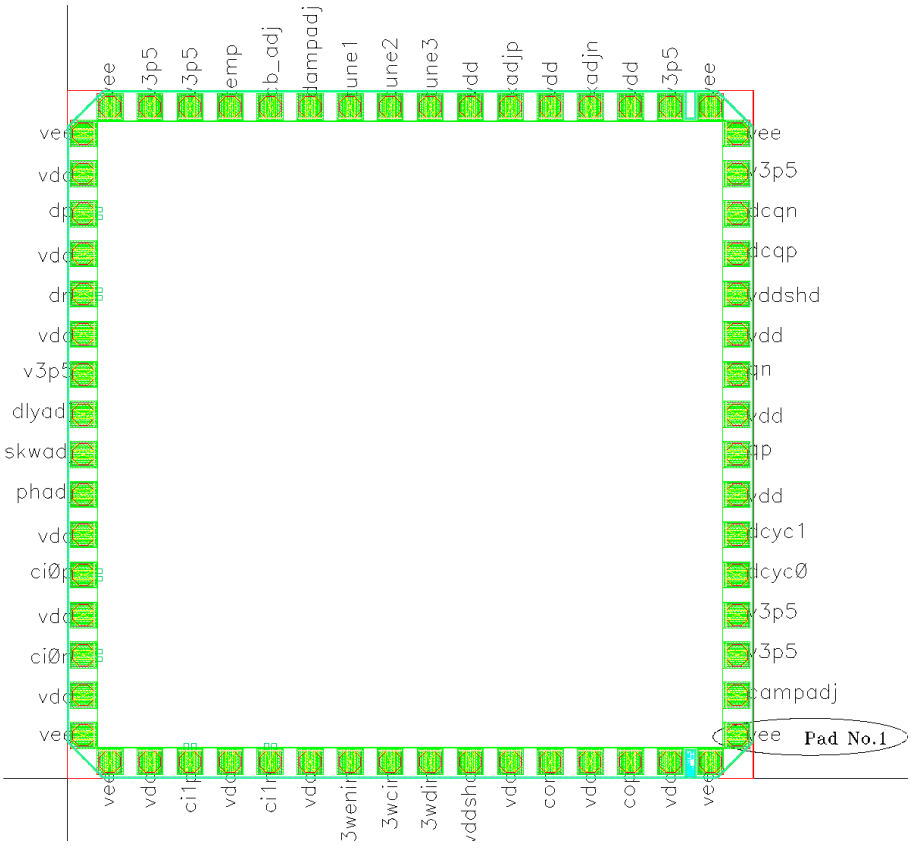
ASNT6111-BD
30*Gbps* Advanced Driver/Amplifier

- High-speed limiting amplifier with selectable built-in pre-emphasis.
- Four pre-emphasis taps with externally controlled weight and inversion.
- Adjustable data output amplitude and eye quality.
- Single-ended output data eye cross point adjustment.
- Optional main clock frequency multiplier by 2.
- Duty cycle indicators for the main clock before and after the multiplier.
- Opposite and parallel adjustment of the main clock and data delays.
- Additional clock input.
- Fully differential CML input and output data and clock interfaces.
- Selectable main or additional clock output with adjustable amplitude.
- CMOS 3-wire interface for digital controls.
- On-chip linear temperature sensor.
- Two power supplies: negative -4.3*V* and floating positive +3.5*V*.
- Power consumption: <4.4*W*.
- Unpackaged bare die.



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DESCRIPTION

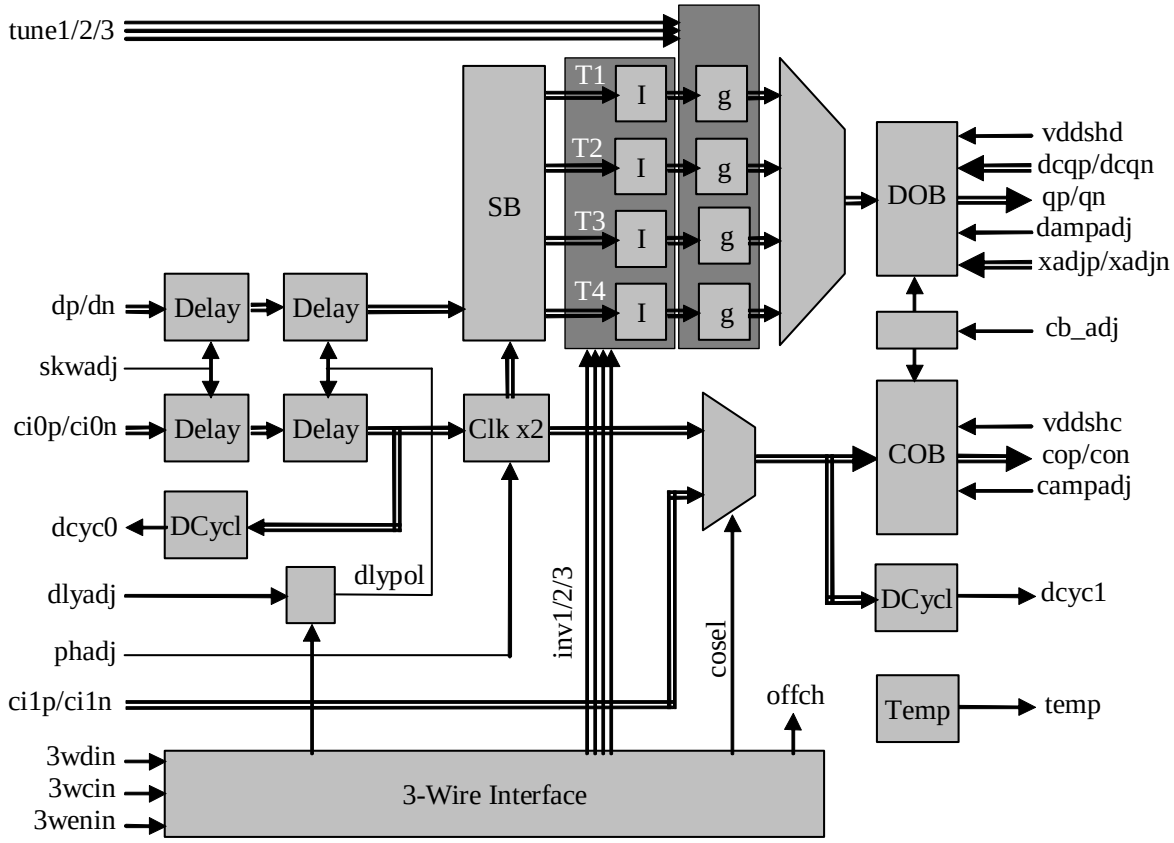

Fig. 1. Functional Block Diagram

The ASNT6111-BD SiGe IC shown in Fig. 1 is an advanced programmable driver amplifier (ADA) with built-in pre-emphasis. ADA generates a combination of four delayed copies of its input differential data signal dp/dn with certain user-controlled weights and polarities. The copies are created in a 4-bit shift register activated by internal high-speed clock signal (see Sampling Block and Taps). This clock signal is a copy of the main input clock ci0p/ci0n with either matching or doubled frequency. In the multiply-by-2 clock mode, the duty cycles of the input and internal clock signals are monitored and the output duty cycle can be adjusted through external control port phadj (see Clock Multiplier).

Input clock and data signals can be delayed in the same or opposite directions to ensure their correct phase relations at the inputs of the shift register and at the chip outputs (see Input Delay Section). ADA can accept one additional clock signal ci1p/ci1n and deliver it to output cop/con instead of the main clock "ci0p/n", thus operating as a clock buffer (see Additional Input Clock and Clock Output Buffer).

The part's I/Os support CML logic interface with on-chip 50*Ohm* termination to ground. External 50*Ohm* termination is required. DC-coupling for data and clock output ports is strongly recommended. The input ports can use DC or AC coupling. Amplitude and peaking in the clock and data output signals can be externally adjusted. Both single-ended data output signals also have controlled DC common-mode levels and eye crossing points (see Data Output Buffer).

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The operational modes of the chip are controlled through a 3-wire serial interface (see 3-Wire Interface Control Block).

The chip operates from one negative power supply (positive pin connected to external Ground, negative pin vee=-4.3*V*) and one floating positive power supply (negative pin connected to vee and positive pin v3p5=3.5*V*). It is recommended to keep the relative deviation of v3p5 from Ground within less than ±0.1*V*.

Input Delay Section

As shown in Fig. 1, ADA accepts differential input data dp/dn and clock ci0p/ci0n signals and inserts them both into identical variable delay blocks Delay that can be oppositely adjusted by external analog control voltage skwadj in order to eliminate skew between the two channels. The blocks can compensate the skew up to ±15*ps*. Subsequently, both input signals are further processed by two additional Delay blocks that can be adjusted in parallel or opposite modes depending on the polarity of internal digital signal dlypol ("0"=parallel, "1"=opposite) provided by the 3-Wire Interface block. This second pair of Delay blocks allows for external adjustment of the data vs. clock signals when operating in opposite mode or varying the delay of the output data and clock signals when in parallel mode. The delay adjustment range is ±75*ps* in the opposite mode or 0-75*ps* in the parallel mode.

Clock Multiplier

The clock doubler Clkx2 uses a "delay and XOR" mechanism to create output clock pulses from each edge of the input clock ci0p/ci0n. The multiplier is intended for operation with input clock signals within the frequency range from 4*GHz* to 15*GHz*. Analog control voltage phadj performs a dual function. Voltages within the range from 0*V* to -2.0*V* activate the multiplication function and are used for tuning the block's internal delay in order to achieve 50% duty cycle of the multiplied clock. Voltages between -2.0*V* and vee disable the multiplication function and allow for direct passing of the input clock to the multiplier's output. This mode should be used for operation with clock signal frequencies below 14*GHz*.

Two duty cycle control blocks DCycl are used for monitoring the clock pulse shapes before and after the multiplier. The first block is positioned before the multiplier and delivers single-ended analog voltage dcyc0 that indicates the input clock's duty cycle deviation from 50%. The second block is positioned after the multiplier and delivers similar signal dcyc1 for the output clock. Both output voltages can be used in combination with phadj input within external control loops for getting an optimal shape of the multiplied clock.

Additional Input Clock and Clock Output Buffer

ADA can also accept an additional input clock signal ci1p/ci1n and deliver it to the clock output. This allows the IC to operate solely as a clock amplifier where the output clock signal's amplitude supplied by output buffer COB can be adjusted using analog signal campadj. The amplitude range is from 0*Vpp* (campadj≤-2.0*V*) to 900*mVpp* (campadj=0*V*) single ended. COB can also be completely disabled by applying campadj voltage between -2.0*V* and vee. Either ci0 or ci1 clock signal can be processed by output buffer COB. Selection of the input clock is accomplished through digital control signal clock select ("0" - ci0, "1" - ci1) delivered by the 3-wire interface block.

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Quality of the output signal shape can be optimized using control voltages cb_adj and vddshc. The first voltage controls the default position of the output eye crossing point and peaking on the rising edge of the output signal (weak influence). The allowed voltage range is from 0*V* to vee. The second (positive) voltage controls peaking on the falling edge of the output signal (strong influence). The allowed voltage range is from 2.8*V* to 4.3*V* with the negative pin of the supply connected to vee. In both cases, more positive voltages correspond to more peaking.

Sampling Block and Taps

Sampling block SB is essentially a 4-bit shift register that generates 4 delayed bits T1-T4 needed for ADA's 4-tap pre-emphasis capability. As stated above, analog control voltage dlyadj is used to adjust the phase relationship between clock and data to ensure optimum sampling in SB. All four samples delivered by SB can be independently inverted by circuit blocks I, where the polarity of the signals is set by four control signals inv0/inv1/inv2/inv3 ("0"=direct, "1"=inverted) provided by the 3-wire interface.

The weights of taps are set by the gain adjustment blocks g that are controlled by a special current distributing circuitry using three external analog voltages tune1/tune2/tune3. The circuitry operates in such a way that the first control voltage tune1 either defines the fraction of the main current that is used in the first tap (0*V* corresponds to full current and -2.0*V* corresponds to no current), or disables the first tap completely (voltages below -2.0*V*). The remaining current is distributed between the second and the third taps in the same way in accordance with the value of the second control voltage tune2, and then between the third and the fourth taps in accordance with the value of the third control voltage tune3. Thus, the total current (and weight) is independent from the number of activated taps and their individual settings. High value (~0*V*) of a certain tuneX signals can be used for disabling all subsequent taps based on internal thresholds. This function can be activated/deactivated through digital control signal offch ("0" – thresholds activated, "1" – thresholds deactivated) delivered by the 3-wire interface block. The combined current from the taps is delivered to data output buffer DOB for the final signal conditioning.

Data Output Buffer

Data output buffer DOB includes several features to tune the output data signal generated by ADA. Similar to COB, adjustment of the output data's amplitude is possible by means of external analog control voltage dampadj. The amplitude range is from 0.0*Vpp* (dampadj≤-2.0*V*) to 1.3*Vpp* (dampadj=0*V*) single-ended.

Differential analog control voltage xadjp/xadjn can be utilized to adjust the crossing points in the single-ended output eyes. At the default state of xadjp = xadjn = 0*V*, the crossing points in both direct and inverted eyes should be centered. The crossing points are moving up in the direct output eye and down in the inverted output eye if xadjp = -xadjn > 0, or in the opposite directions if xadjp = -xadjn < 0. The allowed voltage range of ±4.0*V* corresponds to shifts of the crossing points up to ±25% of the eye amplitude.

Quality of the output signal shape can be optimized using control voltages cb_adj and vddshd as described in Clock Output Buffer section above.

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Finally, 1.0*KOhm* resistors are attached to both data outputs qp and qn to provide DC shifting of the output signals. Access to the resistors is through the control pins dcqp/dcqn. The allowable DC voltage that can be applied to those pins is from 0 to vee.

3-Wire Interface Control Block

To reduce the physical number of digital control inputs to ADA, an 8-bit shift register with a 3-wire input interface has been included on chip. The digital control bits applied through 3wdin input are latched in and shifted down the register by negative edges of low-speed clock 3wcin. Write enable signal 3wenin must be set to logic "1" during the data read-in phase and then set to logic "0" to retain the shifted in values after 8 clock periods of 3wcin. All input signals should have voltage levels of $V^{"1"}$=0*V* and $V^{"0"}$=-3.3*V*. The maximum frequency of 3wcin clock is 100*KHz*. Table 1 below maps the input 8-bit word to the internal digital control signals.

Table 1. 3-Wire Interface Bit Map.

Input Digital Data Byte 3wdin	Internal Digital Control Signal
8th Bit (last serial bit)	tap1 inversion ("0"=direct, "1"=inverted)
7th Bit	tap2 inversion ("0"=direct, "1"=inverted)
6th Bit	tap3 inversion ("0"=direct, "1"=inverted)
5th Bit	tap4 inversion ("0"=direct, "1"=inverted)
4th Bit	dlyadj polarity ("0"=parallel, "1"=opposite)
3rd Bit	output clock select ("0"=ci0, "1"=ci1)
2nd Bit	tap thresholds ("0"=enabled, "1"=disabled)
1st Bit (first serial bit)	Not used

Temperature Sensor

A linear temperature sensor is included on chip. Its behavior is illustrated in Fig. 2 below.

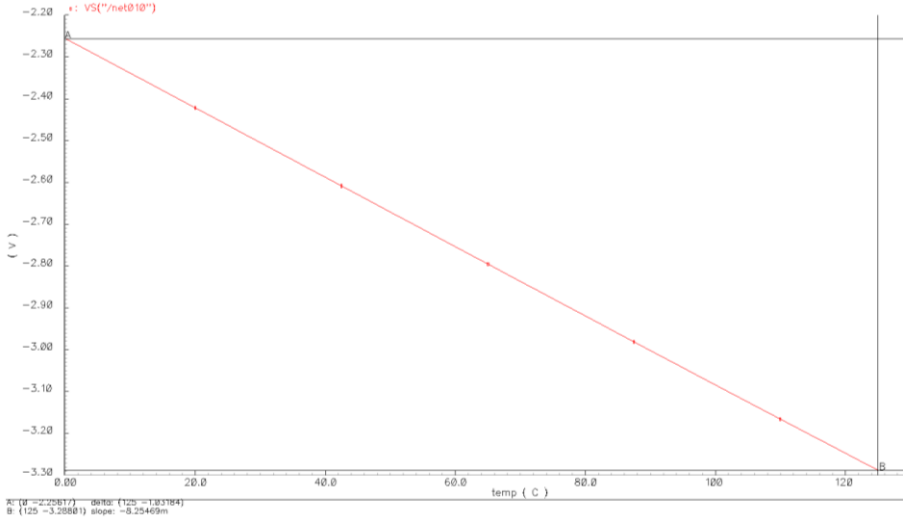

Fig. 2. Temperature Sensor's Characteristic.

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TERMINAL FUNCTIONS

TERMINAL			Description
Name	No.	Type	
High-Speed I/Os			
dp	35	CML Inputs	Differential high-speed data inputs
dn	37		
ci0p	44		Differential high-speed main clock inputs
ci0n	46		
ci1p	51		Differential high-speed additional clock inputs
ci1n	53		
cop	62	CML Outputs	Differential high-speed clock outputs
con	60		
qp	8		Differential high-speed data outputs
qn	10		
Low-Speed I/Os			
3wenin	55	3.3*V* CMOS Inputs	Enable input signal for 3-wire interface
3wcin	56		Clock input signal for 3-wire interface
3wdin	57		Data input signal for 3-wire interface
Analog Control Voltage Inputs			
xadjp	22	Analog Inputs with 100*KOhm* termination to vdd.	Output data eye cross point adjustment, Differential
xadjn	20		
tune3	24		Tap 3 weight adjustment, SE
tune2	25		Tap 2 weight adjustment, SE
tune1	26		Tap 1 weight adjustment, SE
dampadj	27		Data output amplitude adjustment, SE
cb_adj	28		Cascode bias current adjustment, SE
dlyadj	40		Data/clock skew/output phase adjustment, SE
skwadj	41		Data/clock skew adjustment, SE
phadj	42		Clock multiplier delay (output duty cycle) adjustment, SE
campadj	2		Clock output amplitude adjustment, SE
dcqp	13	Analog Inputs	Direct data output common-mode DC shift, SE
dcqn	14		Inverted data output common-mode DC shift, SE
Analog Control Indicators			
temp	29	Analog Outputs	Linear temperature-dependent voltage
dcyc1	6		Linear voltage indicating output clock duty cycle
dcyc0	5		Linear voltage indicating main input clock duty cycle

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Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vdd	External ground	7, 9, 11, 19, 21, 23, 34, 36, 38, 43, 45, 47, 50, 52, 54, 59, 61, 63
vee	-4.3*V* negative power supply	1, 16, 17, 32, 33, 48, 49, 64
v3p5	+3.5*V* floating positive power supply. Negative pin to vee.	3, 4, 15, 18, 30, 31, 39
vddshc	Output clock and data peaking adjustment.	58
vddshd	Positive power supply. Negative pin to vee.	12

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 2. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Negative Supply Voltage (vee)		-4.8	*V*
Positive Supply Voltage (v3p5)		3.8	*V*
Power Consumption		4.8	*W*
RF Input Voltage Swing (SE)		1.2	*V*
Back-of-the-die Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-4.1	-4.3	-4.5	*V*	
vcc		0.0		*V*	External ground
v3p5	3.4	3.5	3.6	*V*	"-" pin to vee
Ivcc		180		*mA*	
Iv3p5		1000		*mA*	
Power		4.3		*W*	
Allowed junction temperature	0	50	100	*°C*	
Data input (dp/dn)					
Rate	DC		30	*Gb/s*	
SE Swing	50	200	500	*mV*	Peak-to-peak
CM Level	vcc-(SE swing)/2				
Clock input (ci0p/ci0n, ci1p /ci1n)					
Frequency	0.1		18	*GHz*	
SE Swing	50	200	500	*mV*	Peak-to-peak
CM Level	vcc-(SE swing)/2				
Data output (qp/qn)					
Rate	DC		28.6	*Gbps*	
SE Swing	0.0		1300	*mV*	Peak-to-peak
CM Level	vcc		vcc-0.65	*V*	
Rise/Fall Times	10	12	14	*ps*	20%-80%
Clock output (cop/con)					
SE Swing, max	600		900	*mV*	Pk-pk, 0-15*GHz*
SE Swing, max	200		650	*mV*	Pk-pk, 15-25*GHz*
SE Swing, max	150		220	*mV*	Pk-pk, 25-28*GHz*
CM Level	vcc		vcc-0.4	*V*	
Rise/Fall Times	10	12	14	*ps*	20%-80%
SE tuning ports (tune1/2/3, skwadj dlyadj phadj dampadj campadj)					
Linear control voltage	-2		0	*V*	
Switch-off threshold		-2		*V*	
Cross point control (xadjp/xadjn)					
Differential voltage range	-8.0		8.0	*V*	±4*V* at each input
CM Level		vcc			
Current into the pin		4		*mA*	at +4*V*
Current out of the pin		-4		*mA*	at -4*V*
Bias control (cb_adj)					
Voltage range	vee		vcc	*V*	
DC common mode voltage control (dcqp/dcqn)					
Voltage range	vee		vcc	*V*	

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PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Variable supply voltages (vddshc, vddshd)					
Voltage range	2.8		4.3	*V*	"-" pin to vee
I_{vddshd}		18		*mA*	All 4 taps active.
I_{vddshc}		1.1		*mA*	
Duty Cycle Indicator (dcyc0/1)					
Voltage range	-3.3		-0.8	V	
Temperature Sensor (temp)					
Voltage range	-3.3		-2.3	V	
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	-0.2		0.0	V	
Low voltage level	-3.3		-3.1	V	
Clock speed			100	KHz	

DIE INFORMATION

The die is 2.4x2.4*mm* square with 64 octagonal pads. The pad's dimensions are 80x80μm^2 with an opening of 74x74μm^2. The pads are placed in 4 groups, 16 pads per chip side with a pitch of 140μm. The substrate of the die is electrically connected to vee.

The part's identification label is ASNT6111-BD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash indicate the bare die version of the product.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.4.1	10-2012	Corrected control voltage range for vddshC and vddshD
1.3.1	10-2012	Corrected description. Corrected electrical characteristics.
1.2.1	08-2012	Corrected temperature information
1.1.1	08-2012	Updated format
1.0.1	08-2012	First release