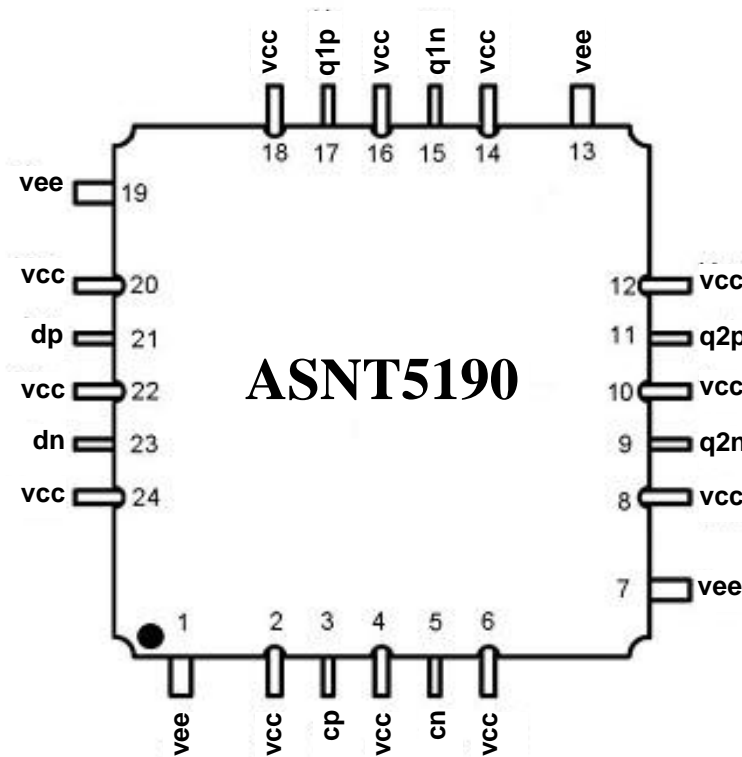


## ASNT5190-KMC

### DC-60Gbps Broadband Digital 1:2 Demultiplexer

- High speed broadband 1:2 Demultiplexer
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 560mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



## DESCRIPTION

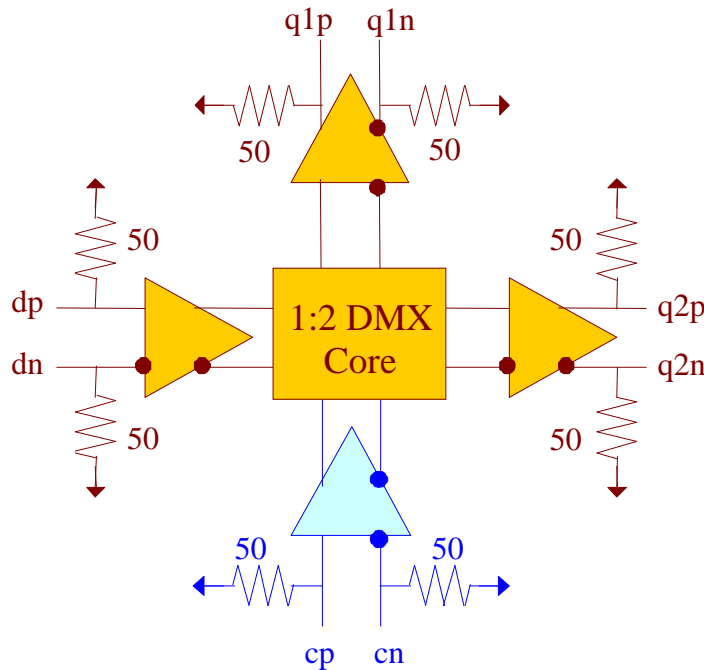


Fig. 1. Functional Block Diagram

The temperature stable ASNT5190-KMC SiGe IC can be utilized as a high speed 1:2 demultiplexer, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can receive a high speed differential data input signal  $dp/dn$  and effectively demultiplex it into two high speed differential data output signals  $q1p/q1n$  and  $q2p/q2n$  by using a high speed differential clock input signal  $cp/cn$ .

The part's I/O's support the CML logic interface with on chip  $50\Omega$  termination to  $vcc$  and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply ( $vcc = 0.0V = \text{ground}$  and  $vee = -3.3V$ ), or positive supply ( $vcc = +3.3V$  and  $vee = 0.0V = \text{ground}$ ). In case of the positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume  $vcc = 0.0V$  and  $vee = -3.3V$ .**



## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.62	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
dp	21	CML input	Differential data input signals with internal 50Ohm termination to VCC
dn	23		
q1p	17	CML output	Differential data output signals with internal 50Ohm termination to VCC
q1n	15		
q2p	11	CML output	Differential data output signals with internal 50Ohm termination to VCC
q2n	9		
cp	3	CML input	Differential clock input signals with internal 50Ohm termination to VCC
cn	5		
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0V or -3.3V)		1, 7, 13, 19



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
Ivee		170		mA	
Power consumption		560		mW	
Junction temperature	-40	25	125	°C	
<b>HS Input Data (dp/dn)</b>					
Data rate	DC		60	Gbps	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
<b>HS Input Clock (cp/cn)</b>					
Frequency	DC		30	GHz	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
Duty cycle	45	50	55	%	
<b>HS Output Data (q1p/q1n, q2p/q2n)</b>					
Data rate	DC		30	Gbps	
Logic "1" level		vcc		V	
Logic "0" level		vcc-0.4		V	With external 50Ohm DC termination
Rise/Fall times	6	8	10	ps	20%-80%
Output Jitter			1	ps	Peak-to-peak

## PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vcc plain that is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT5190-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

The IC complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all 6 substances.

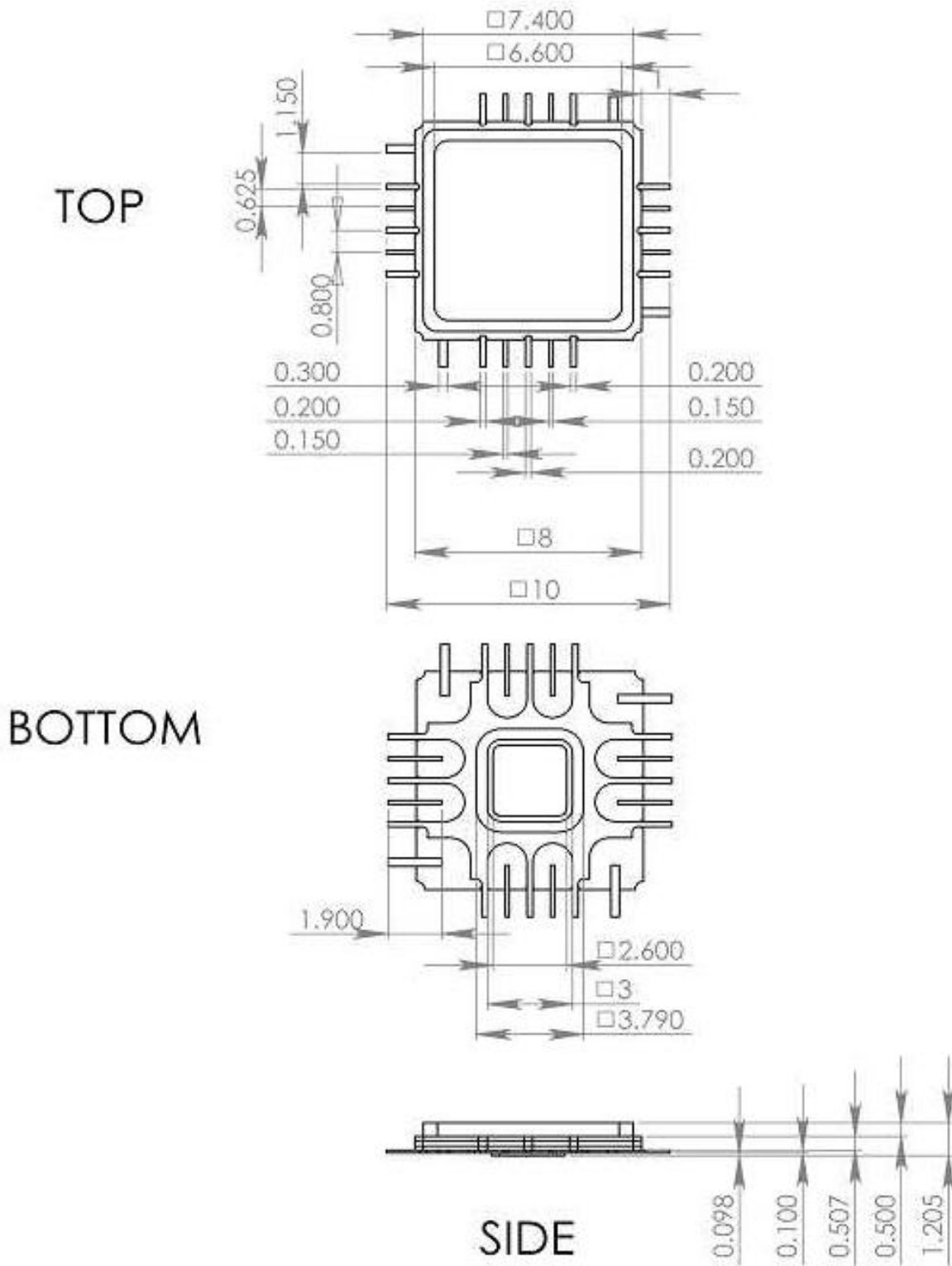


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
2.1.1	03-2013	Revised title Revised electrical characteristics
2.0.1	02-2013	Revised title Added pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Format correction
1.0	10-2008	First release