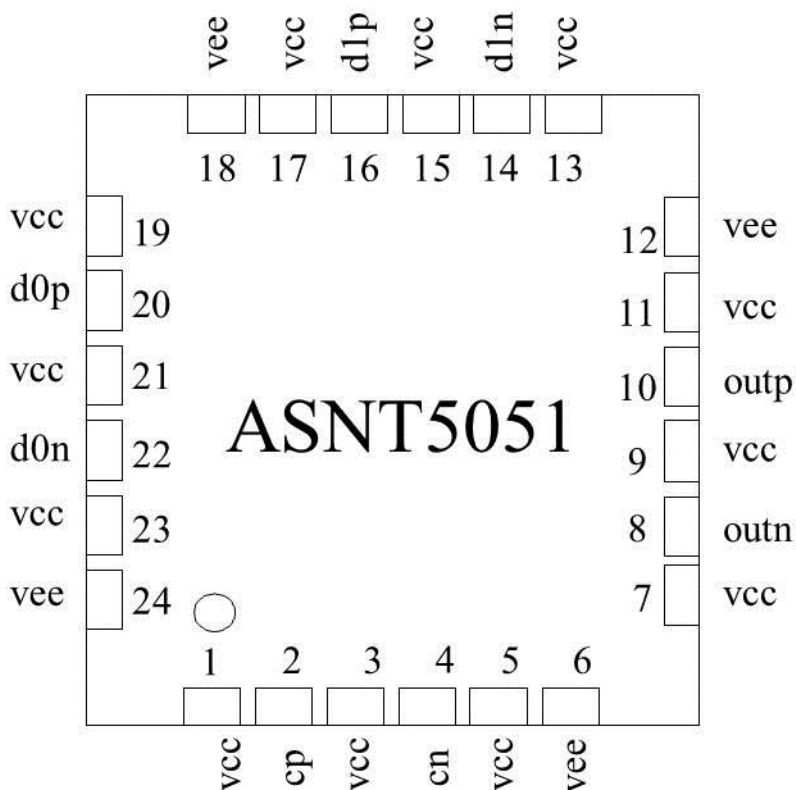# ASNT5051-PQC

DC-32*Gbps*/17*GHz* Broadband 1 of 2 High-Isolation Selector/Switch

- High-speed broadband switch with high isolation for selecting one of two inputs

- Exhibits low jitter and limited temperature variation over industrial temperature range

- DC to 1.0*GHz* analog bandwidth for control input

- Ideal for high speed proof-of-concept prototyping

- Fully differential CML input interface

- Fully differential CML output interface with 400*mV* single-ended swing

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 315*mW*

- Fabricated in SiGe for high performance, yield, and reliability
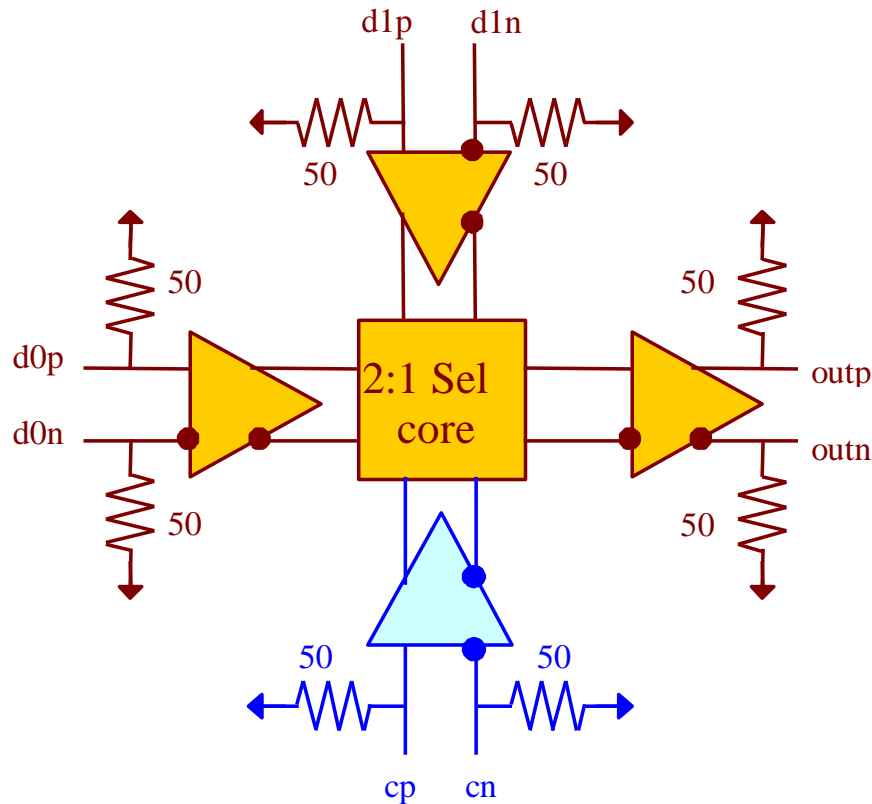
- Standard MLF/QFN 24-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram

The temperature stable and broadband ASNT5051-PQC SiGe IC can be utilized as a high isolation selector switch and is intended for use in high-speed measurement / test equipment. When The IC shown in Fig. 1 can route one of its differential data input signals d0p/d0n or d1p/d1n to its differential output outp/outn while effectively blocking the other data input with high isolation. Selection of a specific data input is achieved through an appropriate external DC biasing of the selector signal inputs cp/cn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.35	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
d0p	20	CML	Differential data input signals with internal SE 50*Ohm* termination
d0n	22	input	to vcc.
d1p	16	CML	Differential data input signals with internal SE 50*Ohm* termination
d1n	14	input	to vcc.
cp	2	CML	Differential select inputs with internal SE 50*Ohm* termination to
cn	4	input	vcc.
outp	10	CML	Differential data output signals with internal SE 50*Ohm* termination
outn	8	output	to vcc. Also require external SE 50*Ohm* termination to vcc.
Supply And Termination Voltages			
Name	**Description**		**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)		1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23
vee	Negative power supply. (0*V* or -3.3*V*)		6, 12, 18, 24

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		95		*mA*	
Power consumption		315		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (d0p/d0n, d1p/d1n)					
Data rate	DC		32	*Gbps*	
Frequency	DC		17	*GHz*	
Swing	50		800	*mV*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		1	*GHz*	
Swing	50		800	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty cycle	40	50	56	*%*	
HS Output Data (outp/outn)					
Data rate	DC		32	*Gbps*	
Frequency	DC		17	*GHz*	
Logic "1" level		vcc		*V*	
Logic "0" level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Rise/Fall times	15		19	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5051-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.
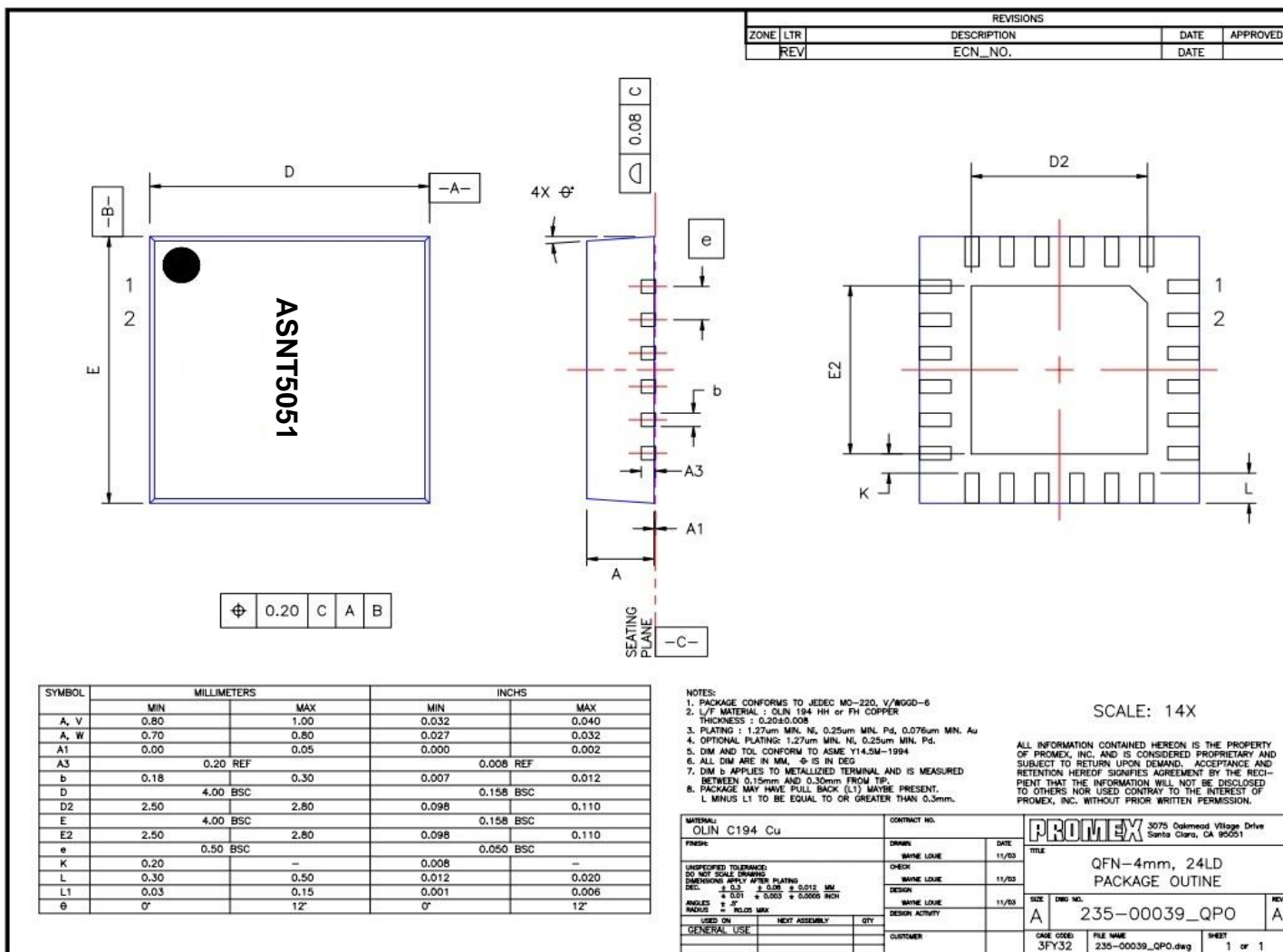
Fig. 2. Package Drawing

REVISION HISTORY

Revision	Date	Changes
1.0.1	03-2013	Initial release