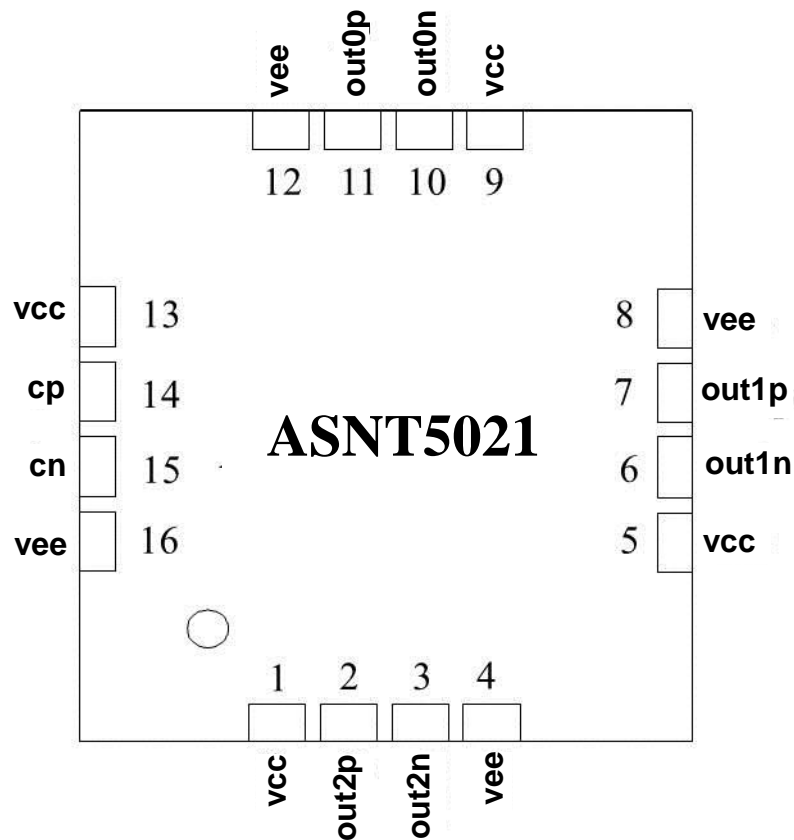




ASNT5021-PQD DC-26Gbps/13GHz Signal Distributor 1-to-3

- High-speed broadband Data/Clock Amplifier and Distributor
- Exhibits low jitter and limited temperature variation over industrial temperature range
- One input differential signal port and three differential amplified output signal ports
- Matched phase delays for all outputs
- Fully differential CML input interface
- Fully differential CML output interfaces with 600mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 780mW
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 16-pin package



DESCRIPTION

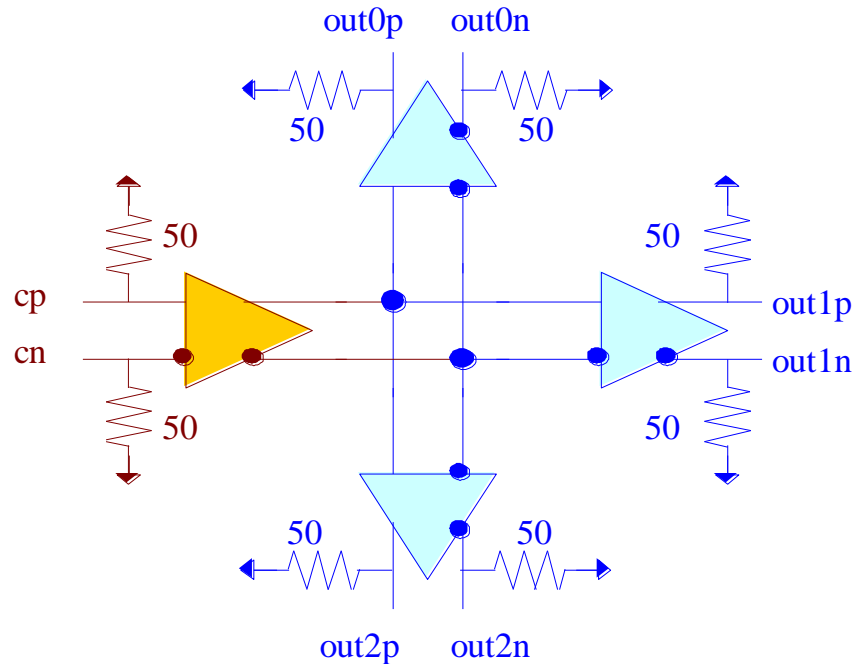


Fig. 1. Functional Block Diagram

The temperature stable ASNT5021-PQD SiGe IC provides active broadband data/clock signal splitting, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can deliver three phase-matched copies of the broadband data/clock input signal *cp/cn* to three high-speed differential outputs *out0p/out0n*, *out1p/out1n*, *out2p/out2n*.

The part's I/O's support the CML logic interface with on chip 50Ω termination to *vcc* and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (*vcc* = 0.0V = ground and *vee* = -3.3V), or positive supply (*vcc* = +3.3V and *vee* = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume *vcc* = 0.0V and *vee* = -3.3V.



ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		0.86	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cp	14	CML input	Differential high speed data/clock inputs with internal SE 50Ohm termination to VCC
cn	15		
out0p	11	CML output	Differential high speed data/clock outputs with internal SE 50Ohm termination to VCC. Require external SE 50Ohm termination to VCC
out0n	10		
out1p	7	CML output	Differential high speed data/clock outputs with internal SE 50Ohm termination to VCC. Require external SE 50Ohm termination to VCC
out1n	6		
out2p	2	CML output	Differential high speed data/clock outputs with internal SE 50Ohm termination to VCC. Require external SE 50Ohm termination to VCC
out2n	3		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		1, 5, 9, 13
vee	Negative power supply (0V or -3.3V)		4, 8, 12, 16



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
v _{ee}	-3.1	-3.3	-3.5	V	±6%
v _{cc}		0.0		V	External ground
I _{vee}		235		mA	
Power consumption		780		mW	
Junction temperature	-40	25	125	°C	
HS Input Data/Clock (cp/cn)					
Data Rate	DC		26	Gbps	
Frequency	DC		13	GHz	
Swing	0.05		1.0	V	Differential or SE, p-p
CM Voltage Level	v _{cc} -0.8		v _{cc}	V	Must match for both inputs
HS Output Data/Clock (out0p/out0n, out1p/out1n, out2p/out2n)					
Data Rate	DC		26	Gbps	
Frequency	DC		13	GHz	
Phase mismatch			2	ps	Between any two SE outputs
Logic "1" level		v _{cc}		V	
Logic "0" level		v _{cc} -0.6		V	With external 50Ω DC termination
Rise/Fall times	13		17	ps	20%-80%
Additive Jitter			5	ps	Peak-to-peak
Duty cycle	45	50	55	%	For clock signal

PACKAGE INFORMATION

The chip die is housed in a standard 16-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the v_{ee} plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5021-PQD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

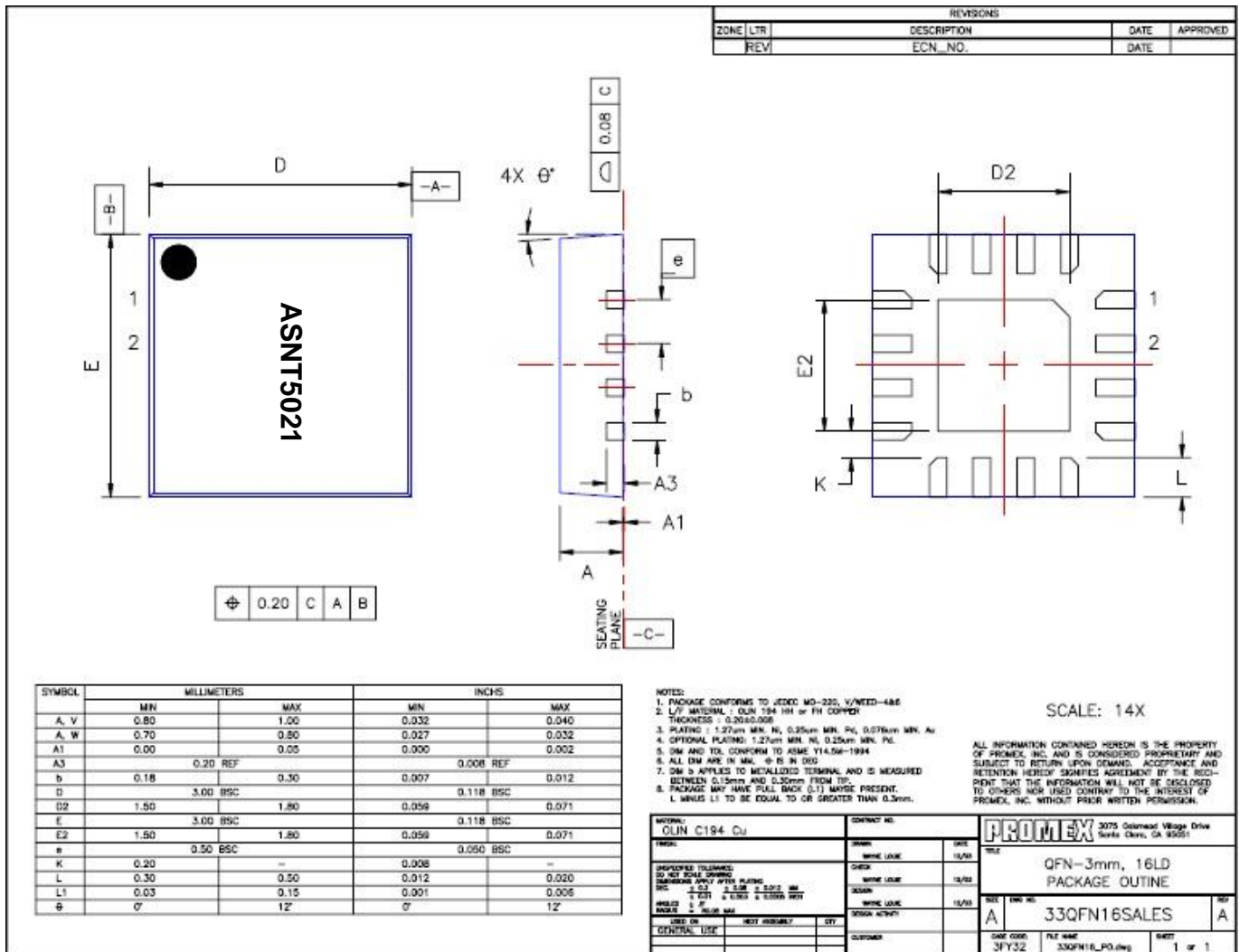


Fig. 2. QFN 16-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
3.1.1	03-2013	Added phase mismatch specifications Revised electrical characteristics table Updated description
3.0.1	02-2013	Revised title Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Revised package information Added mechanical drawing Format correction
2.0	12-2008	Revised electrical characteristics section Revised package information section
1.0	10-2008	Initial release