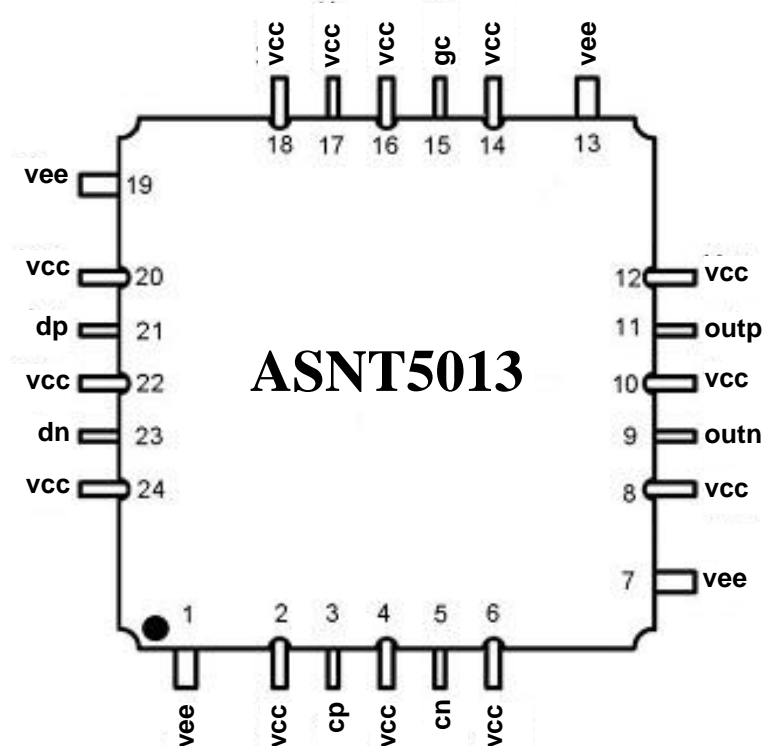




ASNT5013-KMC DC-30Gbps D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock and single-ended output amplitude control
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 6.5ps set-up/hold time capability
- 87% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with amplitude control
- Single +3.3V or -3.3V power supply
- Power consumption: 510mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



DESCRIPTION

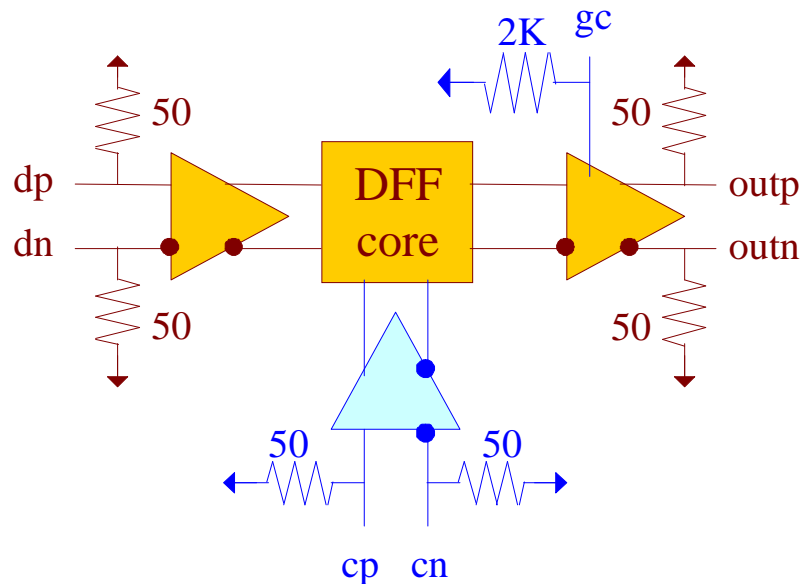


Fig. 1. Functional Block Diagram

The temperature stable ASNT5013-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal *dp/dn* with a full-rate external clock *cp/cn* to create a full-rate retimed NRZ data output *outp/outn* with its output signal amplitude controlled by *gc*.

The part's I/O's support the CML logic interface with on chip *50Ohm* termination to *vcc* and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in



ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply ($v_{cc} = 0.0V = \text{ground}$ and $v_{ee} = -3.3V$), or positive supply ($v_{cc} = +3.3V$ and $v_{ee} = 0.0V = \text{ground}$). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50Ω termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $v_{cc} = 0.0V$ and $v_{ee} = -3.3V$.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum rating shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (v_{ee})		-3.6	V
Power Consumption		0.56	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	21	CML input	Differential data inputs with internal SE 50Ω termination to v_{cc} .
dn	23		



cp	3	CML input	Differential clock inputs with internal SE 500hm termination to VCC.
cp	5		
outp	11	CML output	Differential data outputs with internal SE 500hm termination to VCC. Require external SE 500hm termination to VCC.
outn	9		
gc	15	CML input	Single-ended output amplitude control signal with internal 2KOhm termination to VCC.

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3V or 0)	2, 4, 6, 8, 10, 12, 14, 16, 17, 18, 20, 22, 24
vee	Negative power supply. (0V or -3.3V)	1, 7, 13, 19



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I _{vee}		155		mA	
Power consumption		510		mW	
Junction temperature	-40	25	125	°C	
HS Input Data (dp/dn)					
Data rate	DC		30	Gbps	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		30	GHz	
Swing	0.05		0.8	V	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	V	Must match for both inputs
Clock Phase Margin	85	87	89	%	
HS Output Data (outp/outn)					
Data rate	DC		30	Gbps	
Logic "1" level		vcc		V	
Logic "0" level	vcc-0.7		vcc	V	With external 50Ohm DC termination. Controlled by gc signal
Rise/Fall times			15	ps	20%-80%
Output Jitter			5	ps	Peak-to-peak
Gain Control (gc)					
Control voltage	vcc-1.0		vcc	V	Single-ended

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vcc plain that is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT5013-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

The IC complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all 6 substances.

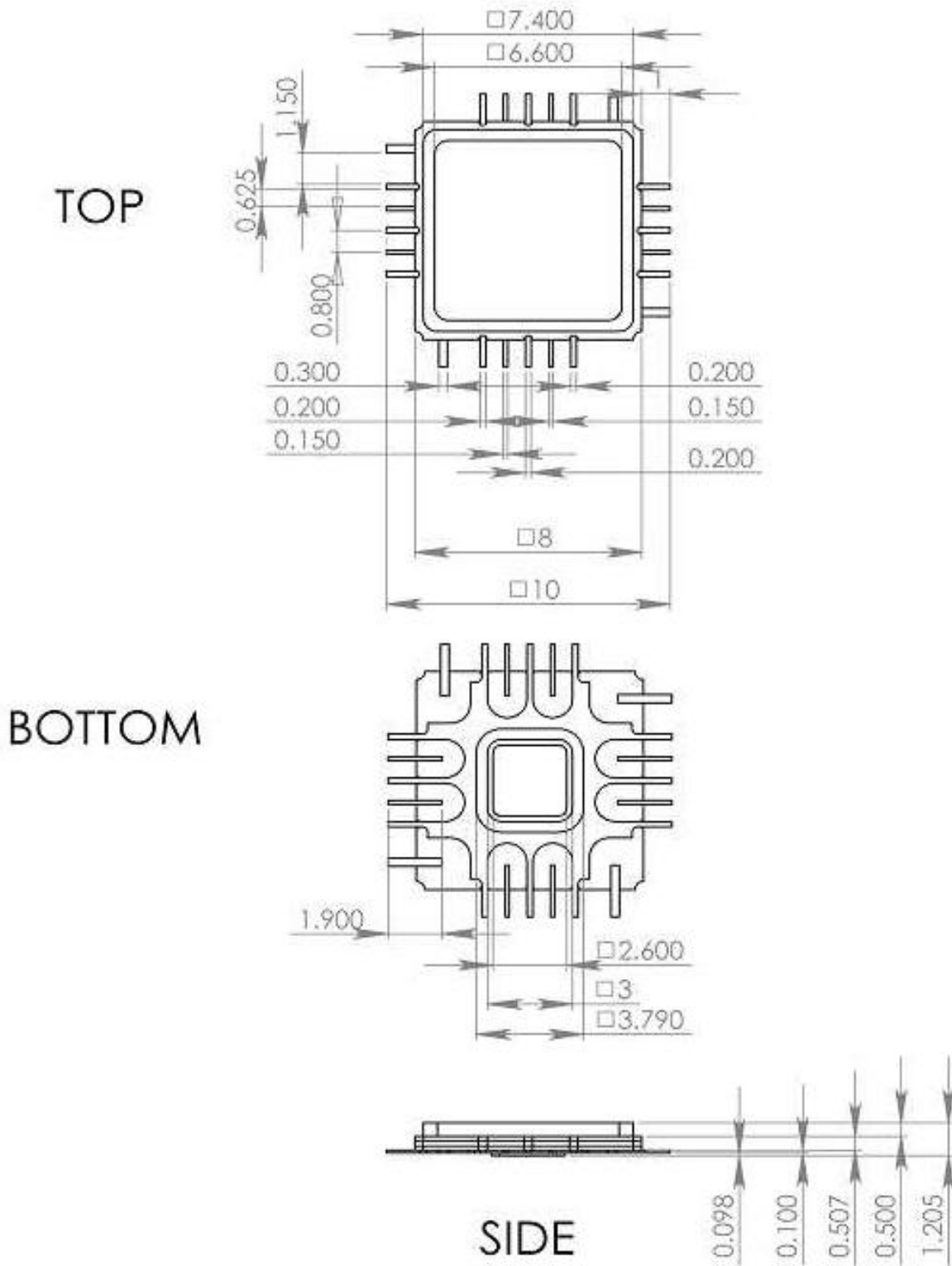


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



REVISION HISTORY

Revision	Date	Changes
3.0.1	02-2013	Revised title Added package pin out drawing Revised functional block diagram Revised description Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
2.0	03-2009	Revised electrical characteristics
1.0	02-2008	First release