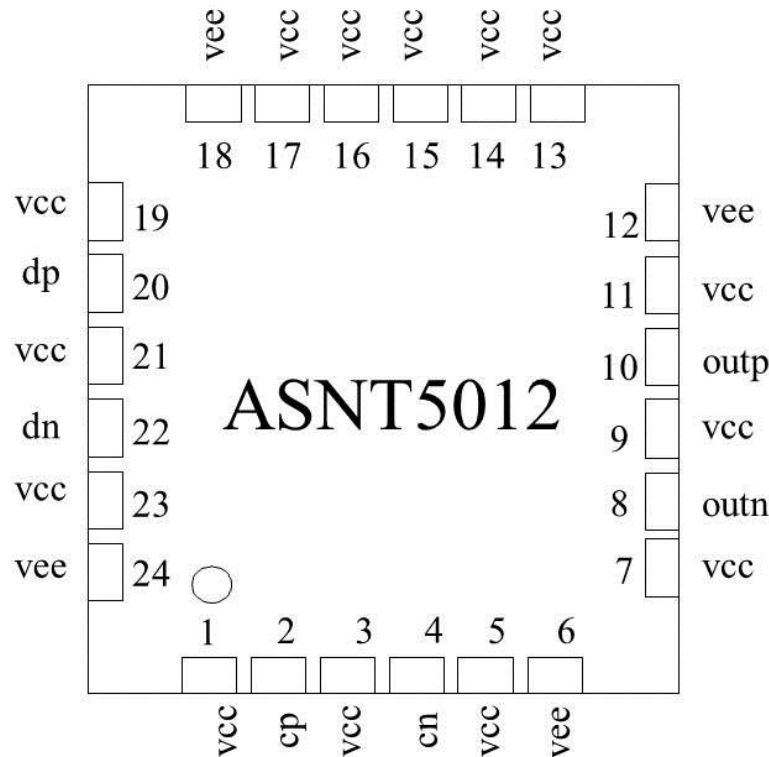




## ASNT5012-PQC DC-17Gbps High Sensitivity D-Type Flip-Flop

- High-speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Sensitive input data buffer with increased common-mode voltage range to support sampling applications
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 8ps set-up/hold time capability
- 89% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 465mW
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



## DESCRIPTION

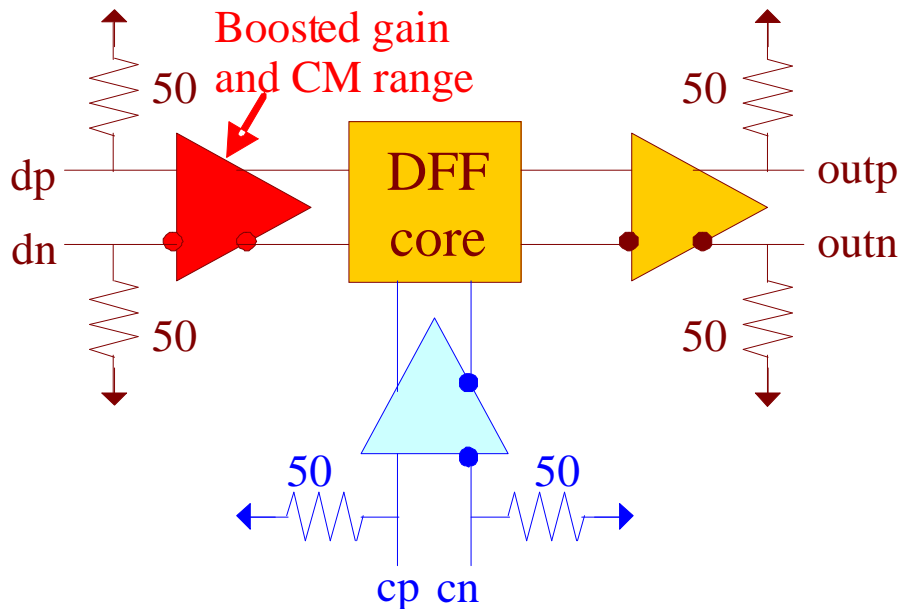


Fig. 1. Functional Block Diagram

The temperature stable ASNT5012-PQC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample the high-speed data signal *dp/dn* with the full-rate external clock *cp/cn* to create the full-rate retimed NRZ data output *outp/outn*.

The data input buffer is designed to have increased input signal sensitivity and is able to operate over a wider range of input common mode (CM) voltages. The part's I/O's support the CML logic interface with on chip *50 Ohm* termination to *vcc* and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (*vcc* = 0.0V = ground and *vee* = -3.3V), or positive supply (*vcc* = +3.3V and *vee* = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with *50 Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.



All the characteristics detailed below assume  $V_{CC} = 0.0V$  and  $V_{EE} = -3.3V$ .

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed  $V_{CC}$ ).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage ( $V_{EE}$ )		-3.6	V
Power Consumption		0.51	W
RF Input Voltage Swing (SE)		1.0	V
Case Temperature		+90	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
dp	20	CML input	Differential data inputs with internal SE 50 $\Omega$ termination to $V_{CC}$ .
dn	22		
cp	2	CML input	Differential clock inputs with internal SE 50 $\Omega$ termination to $V_{CC}$ .
cp	4		
outp	10	CML output	Differential data outputs with internal SE 50 $\Omega$ termination to $V_{CC}$ . Require external SE 50 $\Omega$ termination to $V_{CC}$ .
outn	8		
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	Positive power supply. (+3.3V or 0)		1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 19, 21, 23
vee	Negative power supply. (0V or -3.3V)		6, 12, 18, 24



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
v <sub>ee</sub>	-3.1	-3.3	-3.5	V	±6%
v <sub>cc</sub>		0.0		V	External ground
I <sub>vee</sub>		140		mA	
Power consumption		465		mW	
Junction temperature	-25	50	125	°C	
<b>Input Data (dp/dn)</b>					
Data rate	DC		17	Gbps	
SE swing	25	300	800	mV	Peak-to-peak
CM voltage level	v <sub>cc</sub> -1.5	v <sub>cc</sub> -0.3	v <sub>cc</sub>	V	
<b>Input Clock (cp/cn)</b>					
Frequency	0.1		17	GHz	
Swing	50	300	800	mV	Peak-to-peak
CM voltage level	v <sub>cc</sub> -0.8	v <sub>cc</sub> -0.3	v <sub>cc</sub>	V	
Duty cycle	40	50	60	%	
Clock phase margin	86	88	90	%	For reliable data latching
<b>HS Output Data (outp/outn)</b>					
Data rate	DC		17	Gbps	
Logic "1" level		v <sub>cc</sub>		V	
Logic "0" level		v <sub>cc</sub> -0.4		V	With external 50Ωm DC termination
Rise/Fall times			22	ps	20%-80%
Output Jitter			10	ps	Peak-to-peak

## PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the v<sub>ee</sub> plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5012-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

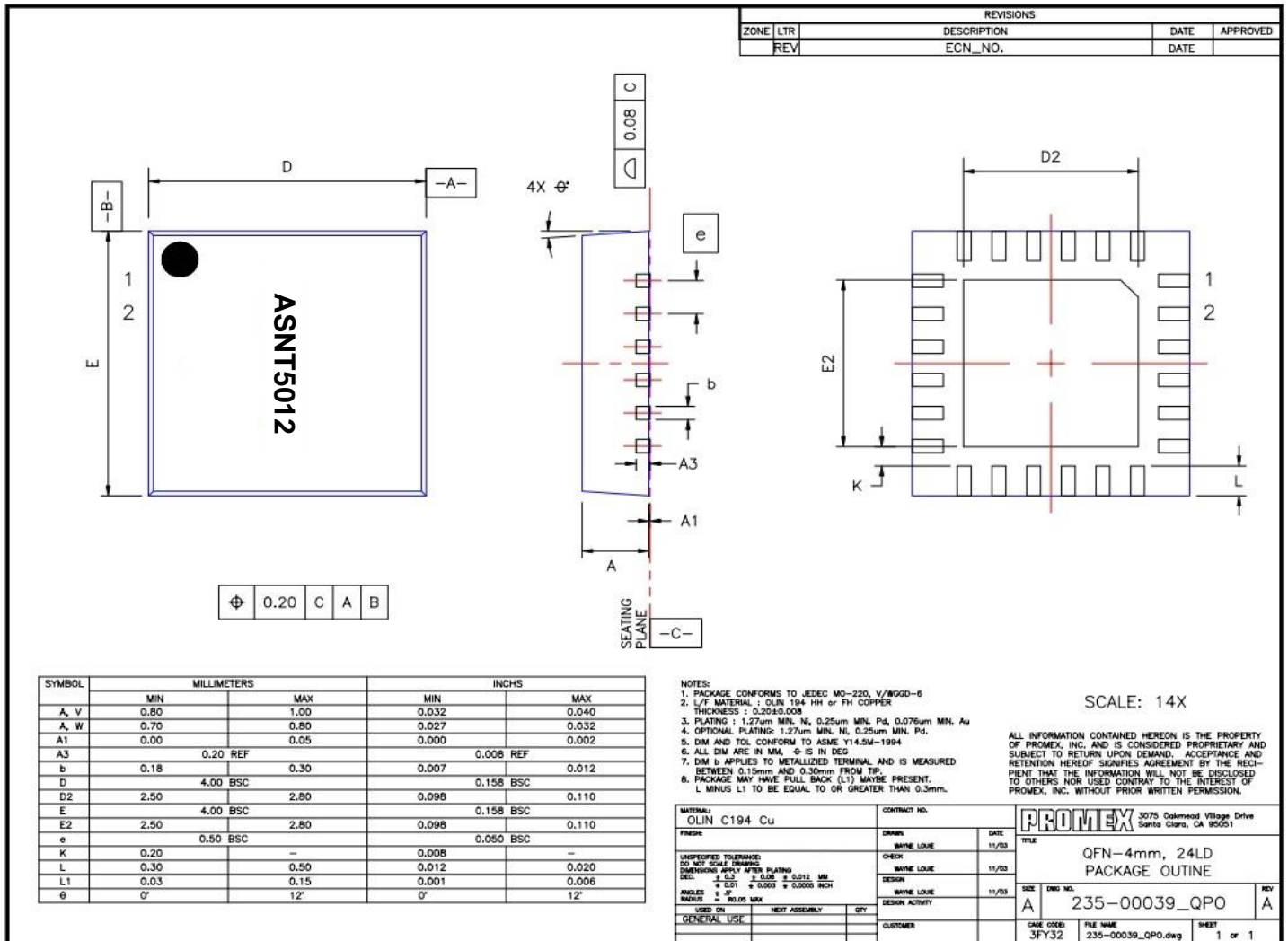


Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
3.2.1	02-2013	Revised title Revised package information
3.1.1	01-2013	Revised maximum speed
3.0.1	01-2013	Revised package pin out drawing Revised functional block diagram Added power supply configuration Added absolute maximum ratings Revised terminal functions Revised electrical characteristics Added package information and mechanical drawing Format correction
2.0	07-2009	Revised electrical characteristics
1.0	02-2008	First release