ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

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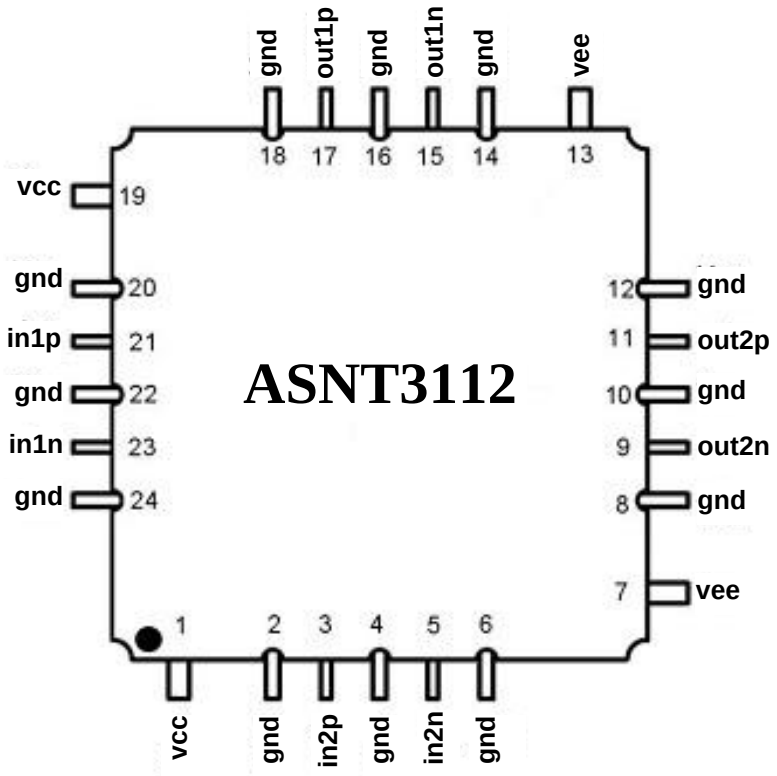
ASNT3112-KMC
DC-32*Gbps* Dual-Channel Linear Signal Level Down-Shifter

- High-speed broadband level down-shifter for analog or digital signals
- Fully differential input CML-type interface with on-chip single-ended 50*Ohm* terminations to the positive supply rail
- Fully differential output CML-type interface with on-chip single-ended 50*Ohm* terminations to ground
- Differential input linearity range up to 800*mV*
- Differential gain of approximately 0*dB*
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fabricated in SiGe for high performance, yield, and reliability
- Power consumption: 1.15*W*
- Custom CQFP 24-pin package



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DESCRIPTION

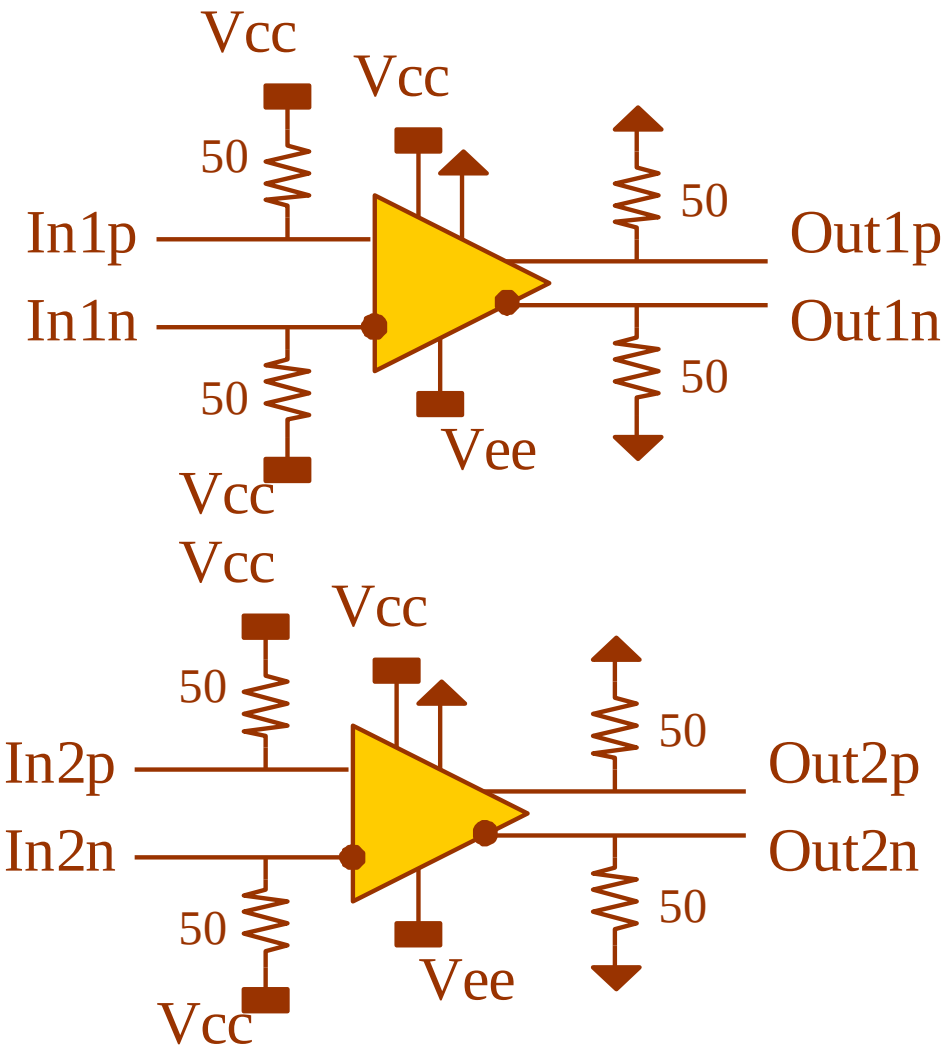

Fig. 1. Functional Block Diagram

The ASNT3112-KMC SiGe IC shown in Fig. 1 provides a voltage shift for high-speed data and clock signals from levels associated with positive power supplies to levels associated with negative power supplies.

The part's inputs support the CML logic interface with on chip 50*Ohm* termination to gnd and may be used differentially, AC/DC coupled, single-ended, or in any combination. In the first mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the second mode, the input termination provides the required common mode voltage automatically. The part's outputs support the PCML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination. The differential DC signaling mode is recommended for optimal performance.

Fig. 2, Fig. 3, and Fig. 4 below demonstrate the chip's simulated performance.

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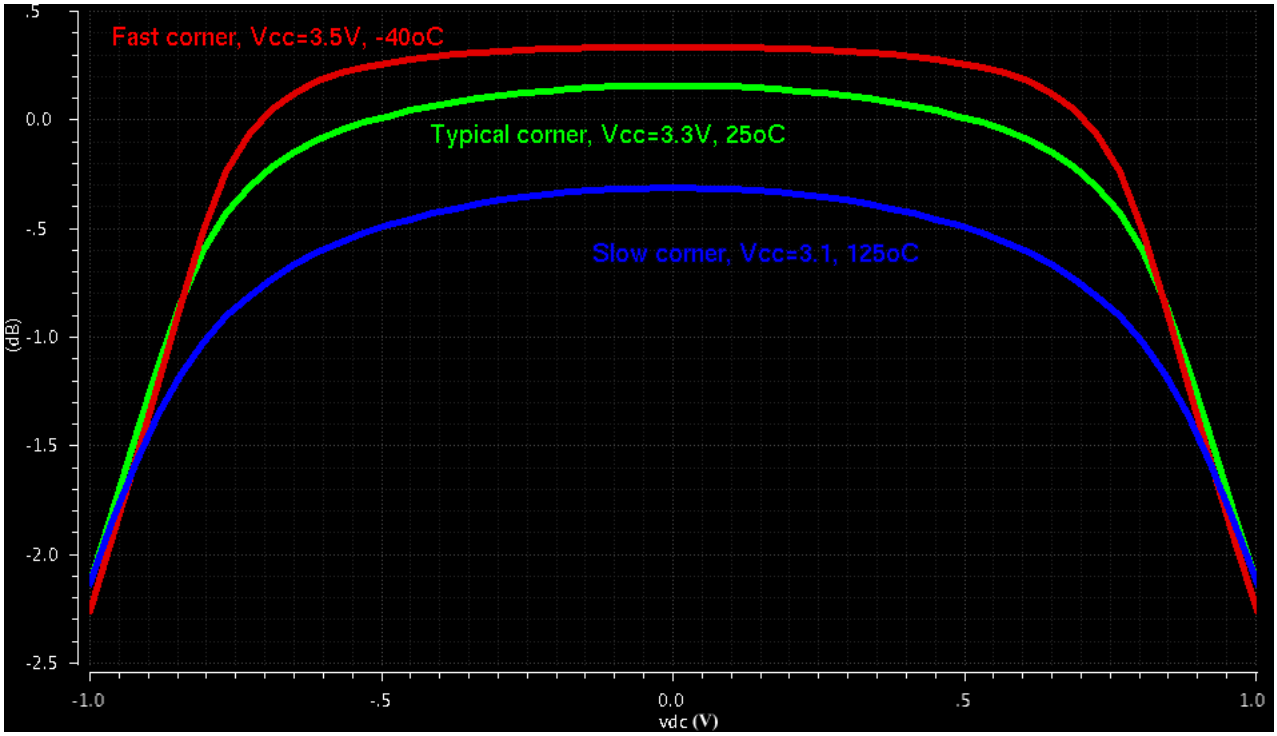

Fig. 2. Simulated DC Amplitude Gain Compression

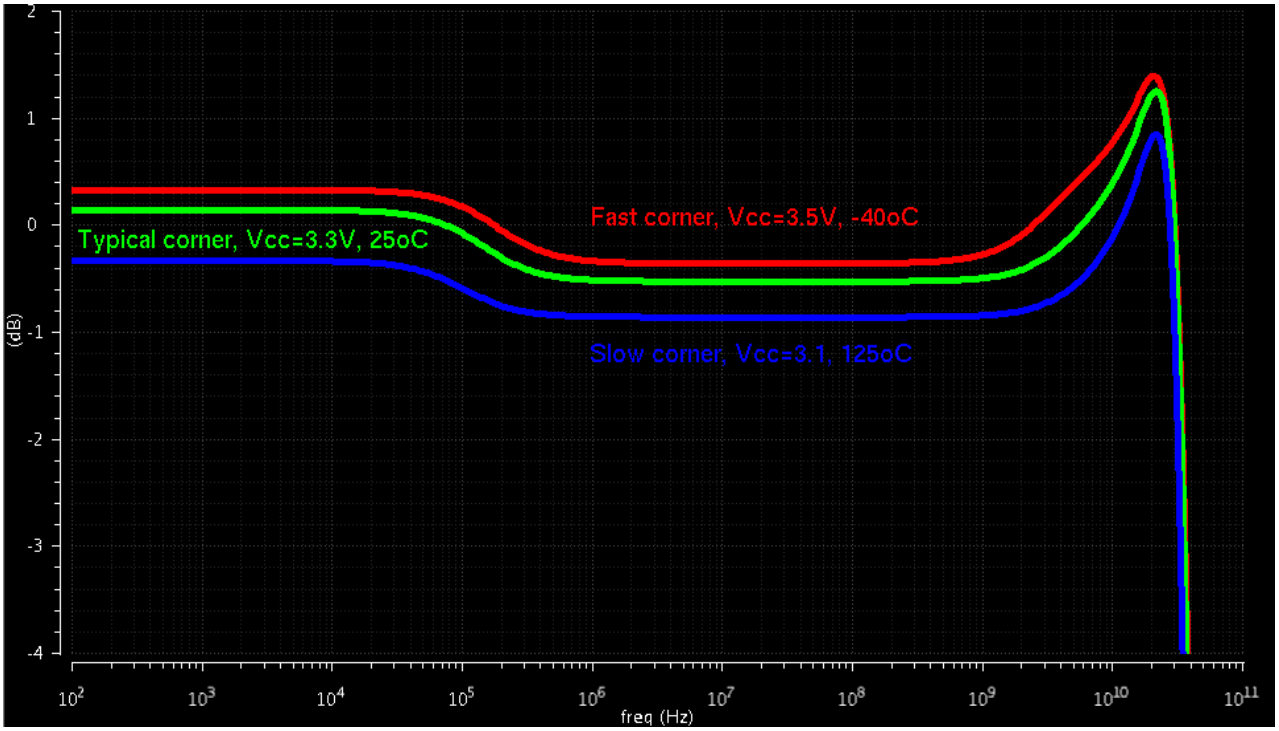

Fig. 3. Simulated Frequency Gain Compression

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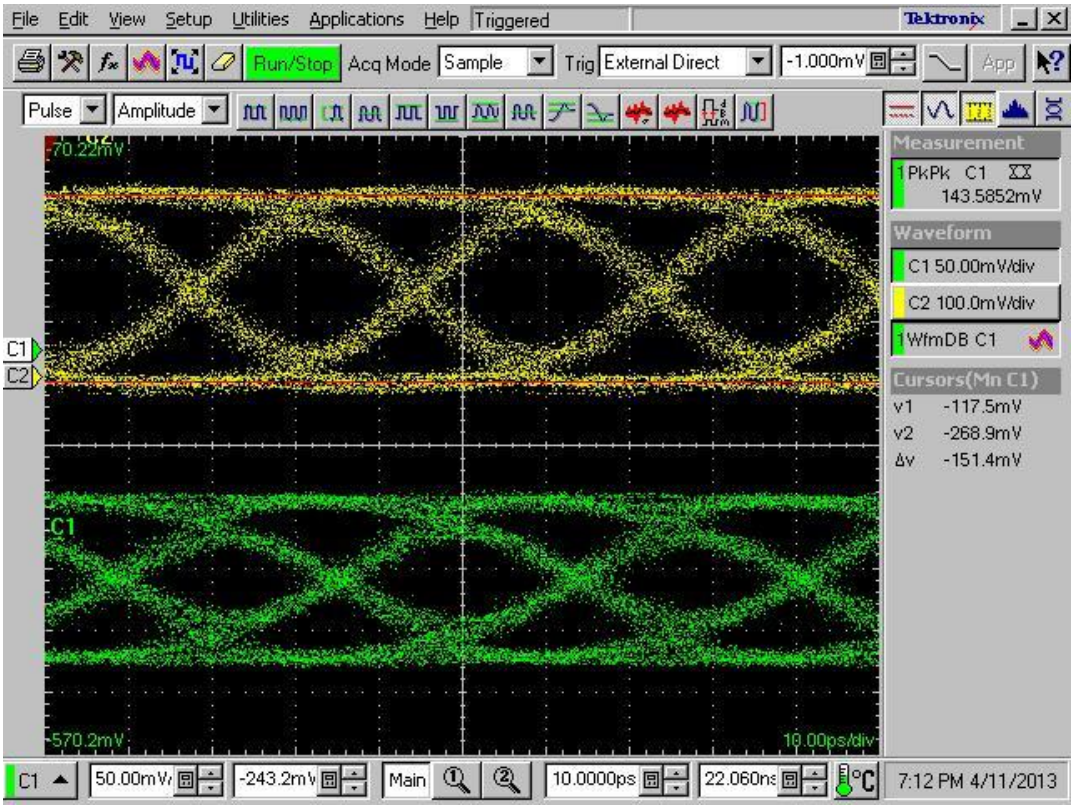

Fig. 4. Eye Diagrams of 36Gbps PRBS 2^7-1 Input (Yellow) and Output (Green) Signals

POWER SUPPLY CONFIGURATION

The chip operates from two independent power supplies related to gnd: negative vee=-3.3*V* and positive vcc=+3.3*V* .

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		1.2	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
in1p	21	CML input	Differential inputs with internal SE 50*Ohm* termination to vcc
in1n	23		
in2p	3	CML input	
in2n	5		
out1p	17	CML output	Differential outputs with internal SE 50*Ohm* termination to gnd. Require external SE 50*Ohm* termination to gnd
out1n	15		
out2p	11	CML output	
out2n	9		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	1, 19
gnd	0*V* external ground	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (-3.3*V*)	7, 13

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
gnd		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	±6%
*I*gnd		210		*mA*	
*I*vcc		135		*mA*	
Power consumption		1150		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (in1p/in1n, in2p/in2n)					
Data rate	DC		32	*Gbps*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Linearity range	800			*mV*	Differential
HS Output Data (out1p/out1n, out2p/out2n)					
Data rate	DC		32	*Gbps*	
Gain		0		*dB*	Differential input and output
CM Level		-375		*mV*	With external 50*Ohm* DC termination
Additive Jitter			<1	*ps*	Peak-to-peak

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PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 5. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to gnd.

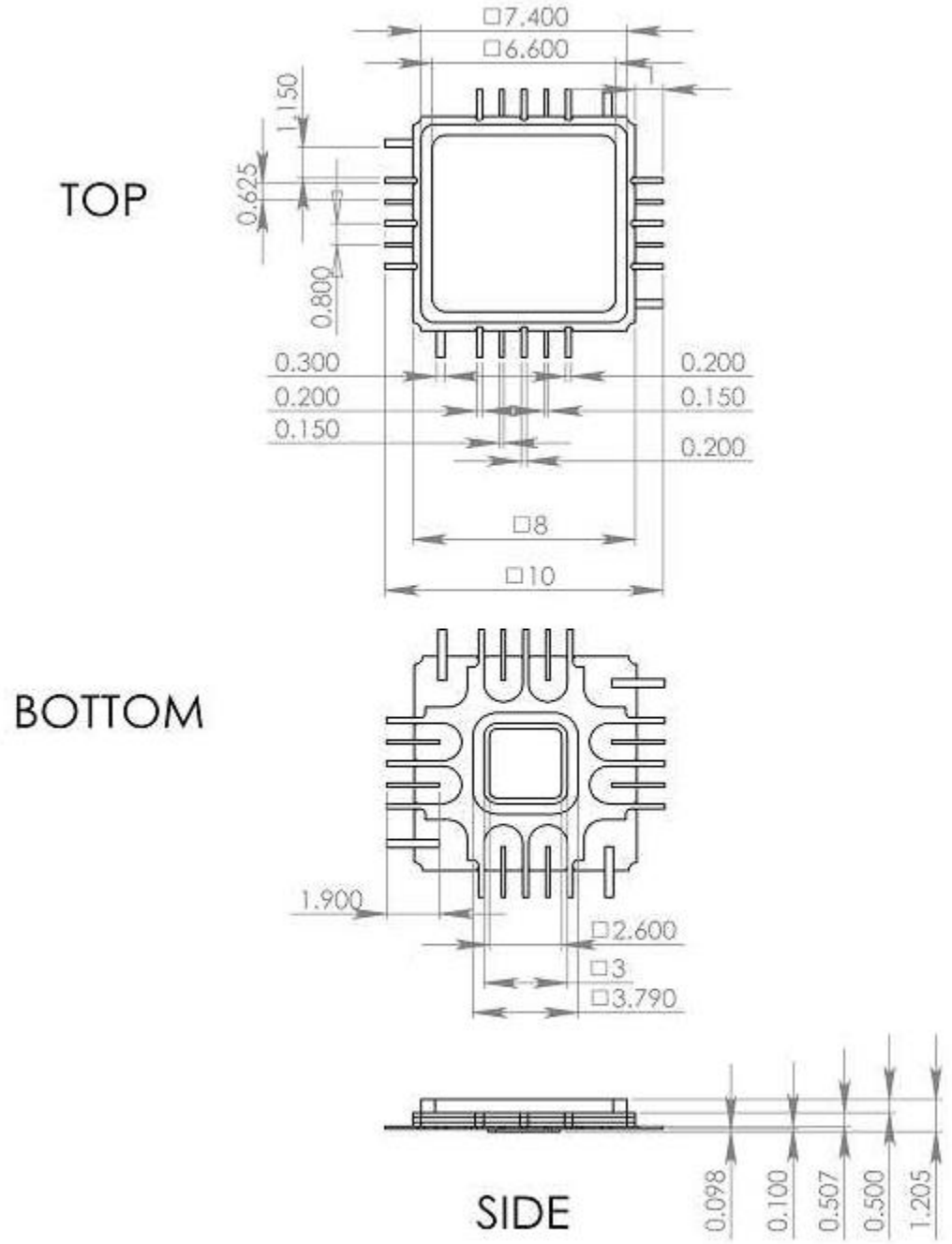

Fig. 5. CQFP 24-Pin Package Drawing (All Dimensions in mm)

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The part's identification label is ASNT3112-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

The IC complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all 6 substances.

REVISION HISTORY

Revision	Date	Changes
1.1.1	05-2013	Inserted measured eye diagram Corrected power consumption specifications Corrected electrical characteristics
1.0.1	03-2013	First release