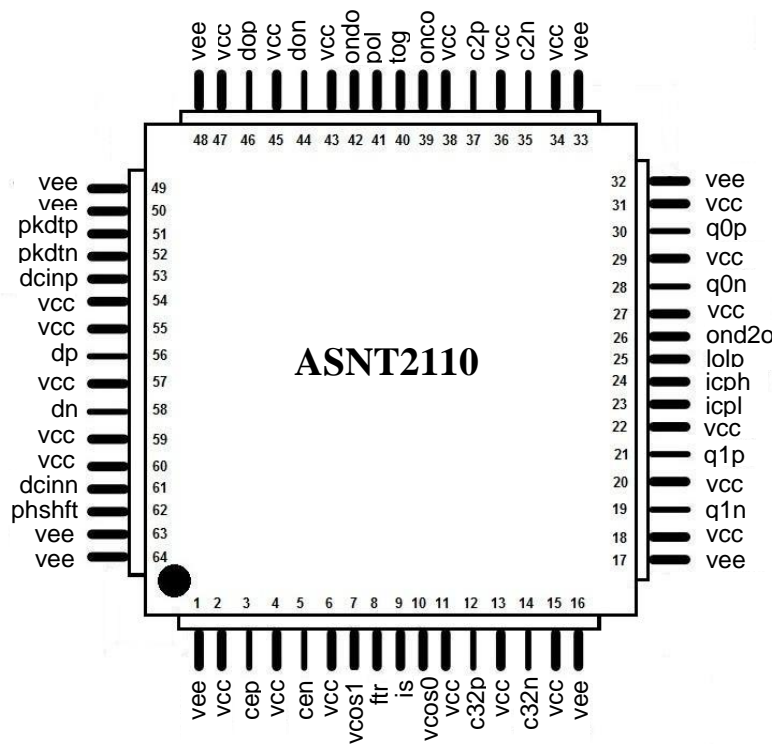




## ASNT2110-KMF Programmable CDR DMUX 1-to-2

- 1:2 demultiplexer (DMUX) with integrated full-rate CDR
- CDR range from 25.5GHz to 32.5GHz covered by 3 selectable VCOs
- Digital operational mode with DC to 32.5GHz external clock
- RZ and NRZ input data formats
- Adjustable time of data sampling point for optimum BER performance
- CML compliant differential input and output high-speed data and clock interfaces
- LVDS compliant input reference clock interface
- Full rate clock and retimed data output for 1:1 CDR operation
- Half rate data outputs with toggle synchronization functionality
- Signal inversion and muting capabilities in all output buffers
- Single +3.3V or -3.3V power supply
- Low power consumption of 1.6W at the maximum operational speed
- Industrial temperature range
- Custom CQFP 64-pin package





## DESCRIPTION

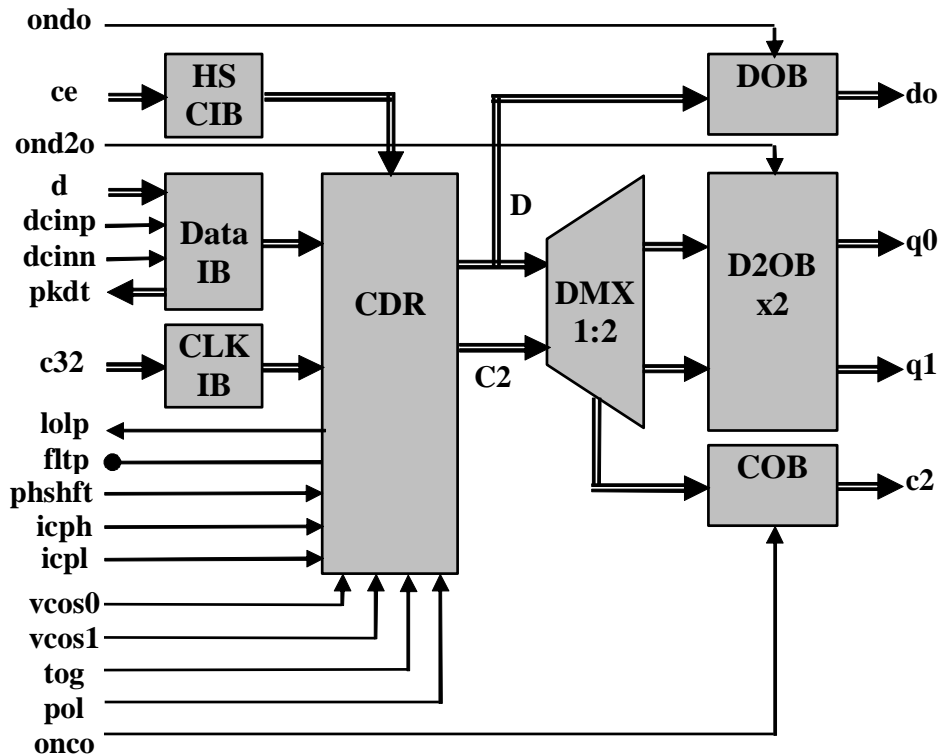


Fig. 1. Functional Block Diagram

ASNT2110-KMF is a 1:2 demultiplexer (DMUX) with full-rate integrated clock and data recovery (CDR). The IC shown in Fig. 1 can function in either CDR mode covering a wide range of input data rates ( $f_{bit}$ ) by utilizing its three on-chip VCOs (voltage-controlled oscillators), or in a broadband digital mode. Selection of the desired working data rate and mode is accomplished through pins **vcos0** and **vcos1** (see Table 1). An external low speed system clock **c32p/c32n** running at 1/32 the frequency of the active VCO must be applied to the low-speed LVDS clock input buffer (CLK IB) in CDR mode. An external full-rate clock **cep/cen** must be applied to the high speed CML clock input buffer (HS CIB) for digital operation.

The main function of the chip is to convert a RZ or NRZ input data signal **dp/dn** with a bit rate of  $f_{bit}$  accepted by CML buffer (Data IB) into 2 parallel NRZ data signals **q0p/q0n** and **q1p/q1n** running at bit rates of  $f_{bit}/2$  and delivered to the outputs by CML data output buffers (D2OBx2). The clock and data are recovered from the input data stream by the CDR. The phase of the clock recovered by the CDR can be adjusted externally through pin **phshft** to locate the optimum data sampling point and achieve the lowest system bit error rate (BER).

A full rate retimed NRZ data output signal **dop/don** is also available through the CML data output buffer (DOB) allowing the part to be used as a 1:1 CDR. Half rate clock **c2p/c2n** delivered through the CML clock output buffer (COB) has a tight phase alignment to the demultiplexed data output signals **q0p/q0n** and **q1p/q1n**.

Data IB can operate with either differential or single-ended input signals. It includes tuning pins **dcinp/dcinn** for DC offset of the input signals in case of AC termination. When the buffer is operating



with a DC-terminated single ended input signal, a correct threshold voltage should be applied to the unused input pin. A peak detector is also included to provide means of demodulating AM components carried by the input data with frequency ranges of up to a few hundred *KHz*. The peak detector's output signal is delivered to the differential port **pkdtp/pkdtm**.

All CML I/Os provide on chip *50Ohm* termination to **vcc** and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). Output buffers **DOB**, **COB**, and **D2OBx2** can be individually disabled through pins **ondo**, **onco**, and **ond2o** to save power.

Utilizing pin **pol**, the deserializer can invert the polarity of the three output data signals. Pin **tog** flips the order of **q0p/q0n** and **q1p/q1n** signals thus simplifying the interface between the DMUX and a following ASIC. It also allows for synchronization of the bit order of two or more DMUXes working in parallel.

A loss of lock CMOS alarm signal **lolp** is generated by the CDR to indicate its locking state. An off chip passive filter is required by the CDR, and should be connected to pin **fr** (see CDR).

The deserializer is characterized for operation from 0°C to 125°C of junction temperature. The package temperature resistance is 15°C/W.

## Data IB

The Data Input Buffer (Data IB) can process an input CML data signal **dp/dn** in either RZ or NRZ format due to its high analog bandwidth. It provides on-chip single-ended termination of *50Ohm* to **vcc** for each input line. The buffer can also accept a single-ended signal to one of its input ports **dp** or **dn** with a threshold voltage applied to the unused pin in case of DC termination. In case of AC termination, tuning pins **dcinp/dcinn** allow for data common mode adjustment. The tuning pins have *1KOhm* terminations to **vcc** and allow the user to change the slicing level before the data is sampled by the recovered clock. Tuning voltages from **vcc** to **vee** deliver *150mV* of DC voltage shift.

Also included in Data IB is an input signal peak detector that delivers its response through the output differential signal **pkdtp/pkdtm**. The detector can demodulate AM component(s) carried by the input data with frequency ranges of up to a few hundred *KHz*. The detector's output impedance is *4KOhm* single ended to **vcc**.

## HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process either differential or single-ended external CML clock signals **cep/cen**. In single-ended mode, the clock is applied to one of the pins together with a threshold voltage applied to the unused pin. The buffer utilizes on-chip single-ended termination of *50Ohm* to **vcc** for each input line.

## CLK IB

The Clock Input Buffer (CLK IB) consists of a proprietary universal input buffer (UIB) that exceeds LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with a speed up to *1Gb/s*, DC common mode voltage variation between **vcc** and **vee**, AC common mode noise with a frequency up to *5MHz*, and voltage levels ranging from 0 to 2.4V. It can also receive a DC-terminated single-ended signal with a threshold voltage between **vcc** and **vee** applied to the unused pin. The input termination impedance is set to *100Ohm* differential.



## CDR

The Clock and Data Recovery Block (CDR) contains both a phase and frequency acquisition loop. The frequency loop works in concert with low-speed clock `c32p/c32n` while the phase loop utilizes data signal `dp/dn`. The CDR requires a single off-chip filter shown in Fig. 2 to be connected to pin `ftf`.

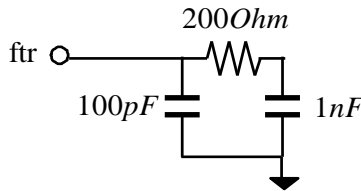


Fig. 2. External Loop Filter

The main function of the CDR is to frequency-lock the selected on-chip VCO to the input data signal (clock recovery) while phase-aligning it to latch in the incoming data with minimal error (data recovery). By default, the CDR aligns the recovered clock's working edge in the middle of the incoming data bits. A DC voltage from `vee` to `vcc` applied to pin `phshft` can be utilized to shift this position from one edge of the data bit to the other in order to locate the optimum sampling point which provides the lowest system BER. The recovered clock is divided down in frequency by two (`C2`) and utilized by DMX 1:2 for demultiplexation of the recovered data.

By utilizing the 2.5V CMOS control pins `vcos0` and `vcos1`, the desired working frequency of the CDR can be selected in accordance with Table 1 below.

Table 1. CDR Mode Selection (Case Temperature from 0 to 90°C)

<b>vcos0</b>	<b>vcos1</b>	<b>VCO Operation Frequency (GHz)</b>
"0" (0V)	"0" (0V)	$f_{min} \leq 25.5, f_{max} \geq 28.0$
"0" (0V)	"1" (2.5V)	$f_{min} \leq 27.5, f_{max} \geq 29.5$
"1" (2.5V)	"0" (0V)	$f_{min} \leq 29.0, f_{max} \geq 32.5$
"1" (2.5V)	"1" (2.5V)	Digital Mode, default state

The loop gain can be adjusted by two 2.5V CMOS control pins `icph` and `icpl` that control the charge pump current as shown in Table 2.

Table 2. Charge Pump Current Control

<b>icph</b>	<b>icpl</b>	<b>Charge Pump current, mA</b>
"0" (0V)	"0" (0V)	$I_{max}$
"0" (0V)	"1" (2.5V)	$I_{max}-0.04$
"1" (2.5V)	"0" (0V)	$I_{max}-0.27$
"1" (2.5V)	"1" (2.5V)	$I_{max}-0.31$

The lock detect circuitry signals an alarm through the 2.5V CMOS signal `lolp` when a frequency difference exists between an applied system reference clock `c32p/c32n` and a recovered full rate clock divided-by-32 that is greater than  $\pm 1000ppm$ .

Another feature included in the CDR is the ability to simultaneously invert the polarity of all three data outputs through the 2.5V CMOS input pin `pol` (`pol="1"` (default): direct; `pol="0"`: inverted). The order of the half-rate output data streams can be inverted by using the 2.5V CMOS input pin `tog`, which provides



means to synchronize two adjacent DMUXes operating in parallel. The synchronization process may be accomplished by the “blind” toggling in one of the chips and leaving the task of recognizing the “right” position to downstream components (e.g. FEC chip).

## DMX1:2

The 1 to 2 Demultiplexer (DMX1:2) latches in the retimed data stream D from the CDR on both edges of the half rate clock signal C2. The high speed data signal is subsequently demultiplexed into two half rate NRZ data signals and delivered to D2OBx2 in parallel fashion as a 2-bit wide word with the order defined by the tog signal.

## DOB

The Data Output Buffer (DOB) receives a full rate retimed serial data stream D from the CDR and converts it into a CML output signal dop/don. This CML buffer requires 50Ohm external termination resistors connected between vcc and each output. The buffer can be enabled or disabled by the external 2.5V CMOS control signal ondo (ondo="1" (default): enabled; ondo="0": disabled).

## D2OBx2

The Half Rate Data Output Buffer (D2OBx2) receives two half rate data signals from DMX1:2 and converts them into CML output signals q0p/q0n and q1p/q1n. The buffer requires 50Ohm external termination resistors connected between vcc and each output. The buffer can be enabled or disabled by the external 2.5V CMOS control signal ond2o (ond2o="1" (default): enabled; ond2o="0": disabled).

## COB

The Clock Output Buffer (COB) receives a half rate clock signal from DMX1:2 and converts it into CML output signal c2p/c2n. The buffer requires 50Ohm external termination resistors connected between vcc and each output. The buffer can be enabled or disabled by the external 2.5V CMOS control signal onco (onco="1" (default): enabled; onco="0": disabled). The negative edge of the c2 signal is aligned to the half rate output data crossing points.

## POWER SUPPLY CONFIGURATION

The ASNT2110-KMF can operate with either a negative supply (vcc = 0.0V = ground and vee = -3.3V), or a positive supply (vcc = +3.3V and vee = 0.0V = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 3.3V and vee = 0V (external ground)**

## TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	Description	Pin Number
vcc	Positive power supply (+3.3V)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vee	Negative power supply (GND or 0V)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64



TERMINAL			DESCRIPTION	
Name	No.	Type		
<b>High-Speed I/Os</b>				
cep	3	Input	CML differential full rate clock inputs with internal SE 50Ohm termination to VCC	
cen	5			
q1p	21	Output	CML differential half rate data outputs. Require external SE 50Ohm termination to VCC	
q1n	19			
q0p	30			
q0n	28			
c2p	37	Output	CML differential half rate clock outputs. Require external SE 50Ohm termination to VCC	
c2n	35			
dop	46	Output	CML differential full rate data outputs. Require external SE 50Ohm termination to VCC	
don	44			
dp	56	Input	CML differential data inputs with internal SE 50Ohm termination to VCC	
dn	58			
<b>Low-Speed I/Os</b>				
c32p	12	Input	LVDS clock input with internal differential 100Ohm termination	
c32n	14			
pkdtp	51	Output	Peak detector outputs	
pkdtn	52			
<b>Controls</b>				
vcos1	7	LS In., 2.5V CMOS	CDR operational mode selection, see Table 1	
vcos0	10			
is	9			VCO current control (high, default: higher current; low: lower current)
icpl	23			Charge pump current control, see Table 2
icph	24			
ond2o	26			D2OBx2 control (high, default: buffer is on; low: buffer is disabled)
onco	39			COB control (high, default: buffer is on; low: buffer is disabled)
tog	40			Order inversion of output data signals (default: high)
pol	41			Data output signal polarity (high, default: inverted data outputs)
ondo	42			DOB control (high, default: buffer is on; low: buffer is disabled)
lolp	25	LS out, 2.5V CMOS	CDR lock indicator (high: no lock; low: locked)	
dcinp	53	LS IN	Input data common mode voltage adjustment	
dcinn	61			
phshft	62	LS IN	CDR sampling point adjustment	
fttr	8	I/O	External CDR filter connection	



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vcc	+3.0	+3.3	+3.6	V	±9%
vee		0.0		V	
I <sub>vcc</sub>		490		mA	All functions active
Power Consumption		1.6		W	
Junction Temperature	-25	50	125	°C	
Case temperature			75	°C	Recommended value
<b>HS Input Data (dp/dn)</b>					
Data Rate	DC		32.5	Gbps	RZ or NRZ
Swing p-p (Diff or SE)	0.05		0.6	V	at 32.5Gbps
CM Voltage Level	vcc-0.8		vcc	V	
<b>LS Input Reference Clock (c32p/c32n)</b>					
Frequency	796		1016	MHz	
Swing p-p (Diff or SE)	0.06		0.8	V	
CM Voltage Level	vee		vcc	V	
Duty Cycle	40	50	60	%	
<b>HS Output Full Rate Data (dop/don)</b>					
Data Rate	DC		32.5	Gbps	
Logic "1" level		vcc		V	
Logic "0" level		vcc -0.4	vcc -0.3	V	
Jitter		7	8	ps	p-p at 25.6Gbps
<b>HS Output Half Rate Data (q0p/q0n, q1p/q1n)</b>					
Data Rate	DC		16.25	Gbps	NRZ
Logic "1" level		vcc		V	
Logic "0" level		vcc -0.4		V	
Jitter		7		ps	p-p at 12.8Gbps
<b>HS Output Half Rate Clock (CDR Mode) (c2p/c2n)</b>					
Clock Rate	12.75		16.25	GHz	25.5 to 32.5Gbps input
Logic "1" level		vcc		V	
Logic "0" level	vcc -0.4		vcc -0.15	V	
Jitter		5	8	ps	p-p at 12.8GHz
<b>HS Output Full Rate Clock (CDR Mode) (c2p/c2n)</b>					
Clock Rate	12.75		16.25	GHz	12.75 to 16.25Gbps input
Logic "1" level		vcc		V	
Logic "0" level	vcc -0.4		vcc -0.15	V	
Jitter		5	8	ps	p-p at 12.8GHz
<b>Input Data Common Mode Control (dcinp/dcinn)</b>					
Input DC Voltage	vee		vcc	V	
Input Data Voltage Shift	0		-150	mV	Referenced to vcc



Output of Peak Detector (pkdtp/pkdtm)				
Swing p-p (Diff)	-1	1	V	Over full input range
CM Voltage Level	vcc -1.0		V	
Data Sampling Point Adjustment (phsft)				
Input DC Voltage	vcc -1.0	NC	vcc	V
Phase Shift	-15	0	+15	ps
Shift Stability	-2	2		ps
Bandwidth	0.0	100		MHz
	From 0°C to 125°C			
CMOS Control Inputs/Outputs				
Logic "1" level	2.1	2.5		V
Logic "0" level	vee +0.4		V	
Timing Parameters				
c2 to q0 & q1 delay variation	2		ps	Over the full temperature range

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only that are specified in ELECTRICAL CHARACTERISTICS. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.8	V
Power Consumption		1.6	W
Input Voltage Swing (SE)		1.0	V
Case Temperature <sup>*)</sup>		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

\*) - Operating the part at temperatures over this value could/will damage the part. Operating at this temperature or any temperatures above the recommended maximum value specified in ELECTRICAL CHARACTERISTICS does not guarantee correct functionality as is stated above.

## PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 3. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

- The lead's gold plating will be removed per the following sections of J-STD-001D:
  - 3.9.1 Solderability
  - 3.2.2 Solder Purity Maintenance
  - 3.9.2 Solderability Maintenance
  - 3.9.3 Gold Removal





2. The leads will be tinned with Sn63Pb37 solder.

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the VCC plain that is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT2110-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

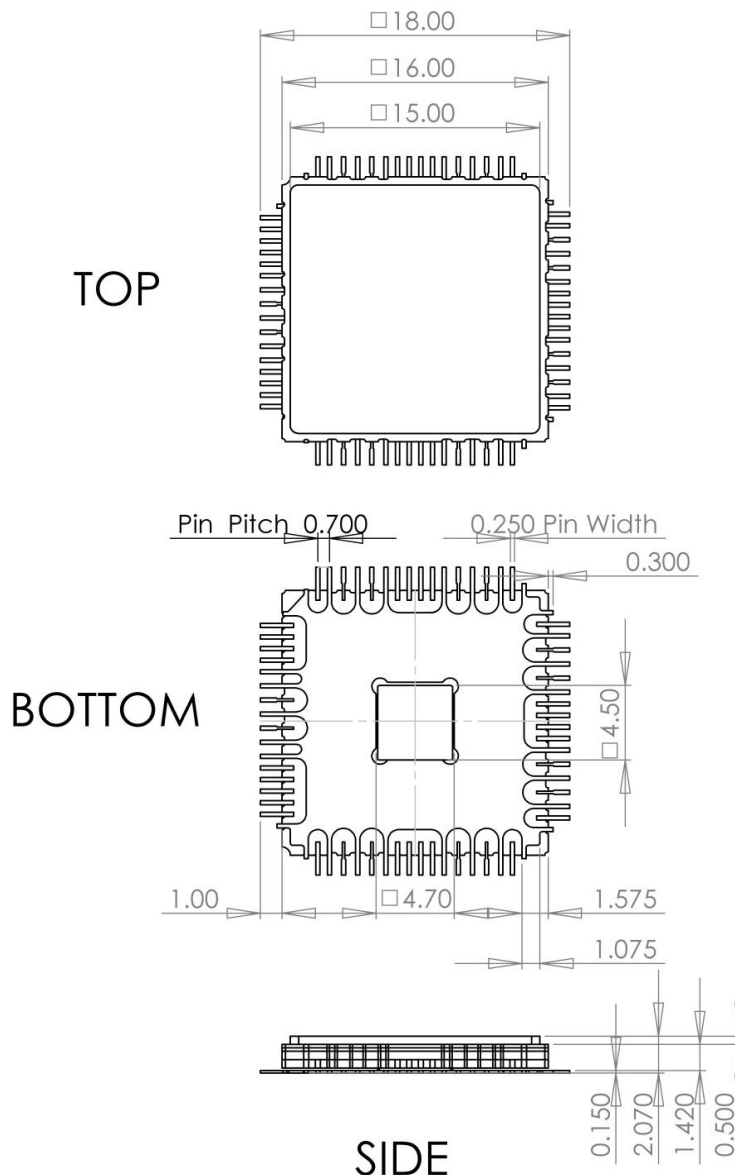


Fig. 3. CQFP 64-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
4.7.1	10-2013	Added recommended case temperature in Electrical Characteristics Added comments in Table 3
4.6.1	09-2013	Added maximum values for the Logic "0" level and jitter of C2
4.5.1	08-2013	Corrected Table 1
4.4.1	08-2013	Table 1: added frequency range Electrical Characteristics: added comments, added full-rate clock, corrected frequency for the input reference clock Corrected format Corrected header
4.3.1	07-2013	Corrected CDR Frequency operating range
4.2.1	06-2013	Corrected CDR Frequency operating range
4.1.1	10-2012	Added supply current Corrected format
4.0	05-2012	Corrected description Added pin out drawing Added loop filter schematic Added description of is, icph, icpl pins
3.3	06-2010	Added additional packaging information Changed package mechanical drawing
3.2	04-2010	Added case temperature
3.1	02-2010	Added absolute maximums rating table Replaced TBDs with values Added RoHS compliancy Added revision history table Revised VCO table Added packaging diagram
3.0	12-2009	Adjusted block diagram Updated center frequencies in VCO table Updated external filter pin assignments Revised packaging information section
2.0	04-2009	Updated center frequencies in VCO table Updated power consumption value
1.0	02-2009	Initial release