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ASNT1016-PQA
16:1 MUX-CMU

- 16 to 1 multiplexer (MUX) with integrated CMU (clock multiplication unit).
- PLL-based architecture featuring both counter and forward clocking modes.
- Supports multiple data rates in the 9.8-12.5*Gb/s* range.
- LVDS, CML, or ECL compatible reconfigurable input data and clock buffers.
- High speed full rate clock output.
- Dual clock-divided-by-16 LVDS output buffers.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 660*mW* at 12.5*Gbps*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

DESCRIPTION

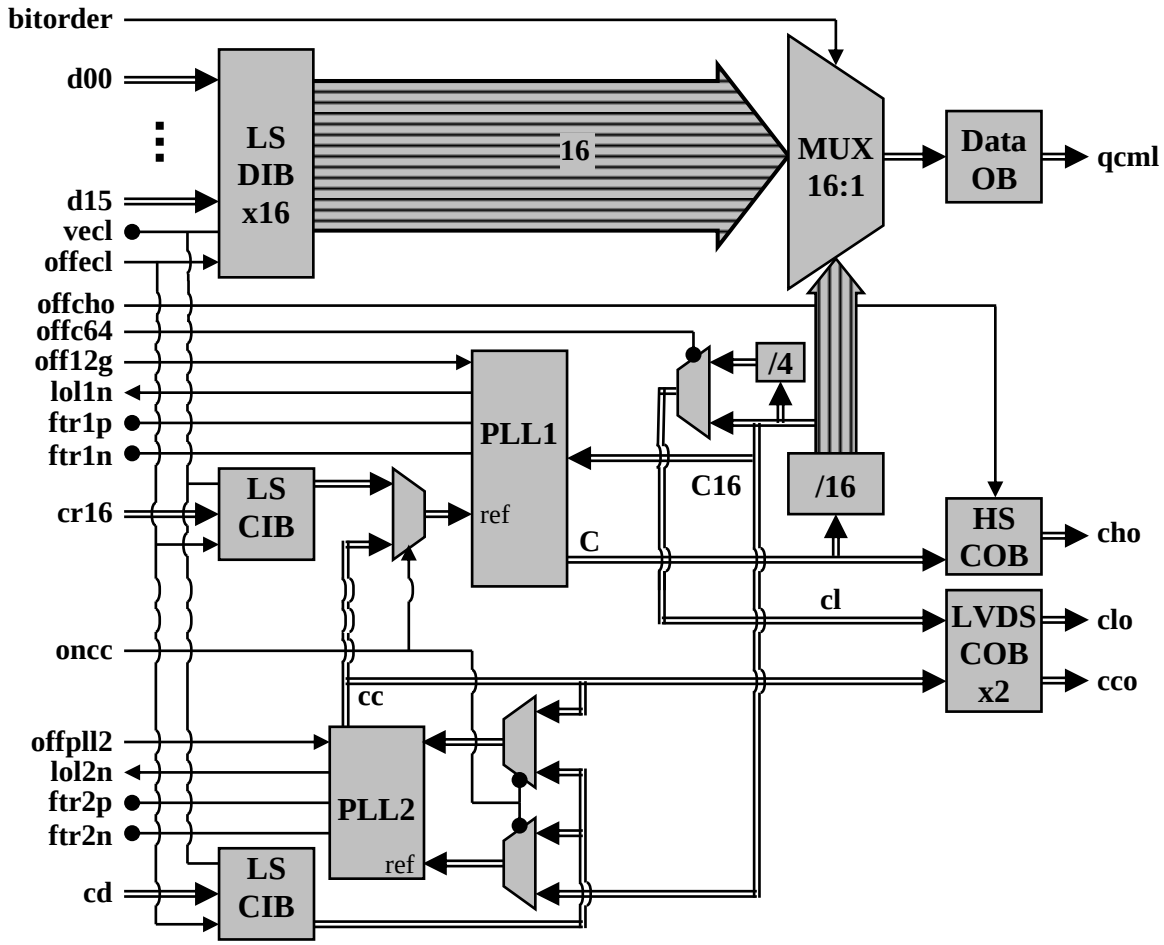

Fig. 1. Functional Block Diagram.

ASNT1016 is a low power and high-speed 16 to 1 multiplexer (MUX) with an internal clock multiplier unit (CMU). The MUX can function at data rates (f_{bit}) between 9.8*Gb/s* to 12.5*Gb/s* by utilizing its multiple on-chip full-rate VCOs.

The main function of ASNT1016 is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high speed serial bit stream running at f_{bit}. It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words "d00"-"d15" through 16 differential inputs with reconfigurable LVDS/CML/ECL interfaces and delivers them to the multiplexers core (MUX16:1) for serialization. The desired input data interface is selected by the CMOS input control signal "offecl" while the proper input termination voltage is provided by "vecl". By utilizing pin "bitorder", the serializer can designate either "d00" or "d15" as the MSB thus simplifying the interface between ASNT1016 and a proceeding ASIC.

MUX16:1 serializes the data words with multiple divided down clock signals that are generated from the full rate clock "C" by the internal divider (/16). The divider also produces a full rate clock divided-by-16 signal "C16" for use by both phase locked loops. "C" is synthesized by the main phase-locked loop (PLL1) that references either an external system level clock "cr16" delivered by one of the low speed clock input buffers (LS CIB) or the internal clock "cc" that is generated by the secondary phase locked loop (PLL2) in concert with a different external low speed clock "cd". Both "cr16" and "cd" must be 1/16 the frequency of the active full rate VCO in PLL1. PLL1 contains 2 full rate VCOs to cover the 9.8-12.5*GHz* range, which are selected utilizing the "off12g" control pin.

ASNT1016 offers 3 different kinds of clocking modes. In the default state, PLL2 is turned off through pin "offpll2" and PLL1 is locked to the "clean" system clock "cr16".

In the forward clocking mode ("offpll2"=0 & "oncc"=0), an active PLL2 is locked to the "dirty" external clock "cd" provided by the preceding ASIC in parallel with the input data and generates a "clean" reference clock "cc" for PLL1. The "clean" system clock "cr16" is not needed since PLL2 provides "clock cleaning" functionality.

In the counter clocking mode ("offpll2"=0 & "oncc"=1), PLL2 is used to ensure a robust interface between the driving ASIC and ASNT1016. PLL1 is locked to the "clean" system clock "cr16", while PLL2 is locked to "C16", which is generated by PLL1 and /16. The low speed output clock from PLL2 "cco" controls the output stage of the preceding ASIC and initiates the transmission of its parallel data and respective clock "cd" across the parallel bus to the inputs of ASNT1016.

The serialized words are transmitted as 2-level signals "qcml" by a differential CML output buffer (Data OB). A full-rate clock "cho" is transmitted by a similar CML buffer (HS COB) in

parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. HS COB may be disabled to save power by means of the 2-state CMOS "offcho" signal. Both output stages are back terminated with on-chip 50*Ohm* resistors.

ASNT1016 also provides a differential low speed output clock derived from PLL1 though a LVDS clock output buffer (LVDS COB). This LVDS output signal "clo" may be configured for either "C16" or full rate clock divided-by-64 "C64" operation through pin "offc64".

Both PLL1 and PLL2 generate loss of lock signal alarms "lol1n" and "lol2n". Off chip capacitors are required for both PLLs and are connected through pins "ftr1p/n" and "ftr2p/n".

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs). UIB is designed to accept differential signals with amplitudes higher than 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative (vee) and positive (vcc) supply voltages, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes of more than 60*mV* p-p and threshold voltages between vee and vcc. By default, the input termination impedance is set to 100*Ohm* differential to support the LVDS standard. Correct impedance for the CML and ECL standards (50*Ohm* single ended to vcc) is set by applying logic "0" to "offecl". Vcc should be applied to "vecl" for CML operation while +*2V* is needed for ECL input signaling.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a UIB that can run at a frequency up to 800*MHz*. This block is used for both low speed clock inputs "cd" and "cr16" inputs and is also affected by the "offecl" and "vecl" control signals.

PLL1

The Main Phase Locked Loop (PLL1) contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filtering capacitor of 1*nF* connected between the pins "ftr1p" and "ftr1n", and two selectable LC-tank VCOs centered at 11.8*GHz* and 11.0*GHz*.

The main function of PLL1 is to synthesize full rate clock "C" by aligning the phase and frequency of "C16" of the activated VCO to the low-speed reference clock signal that is either applied externally "cr16" or generated internally by PLL2 "cc".

A logic "0" output CMOS loss-of-lock "lol1n" alarm signal is generated by PLL1 if its two input clock signals are not matching in phase and/or frequency.

Selection of the different VCOs of PLL1 is achieved by utilizing the CMOS control pin "off12g". A logic "1" chooses the 11.0*GHz* VCO while a logic "0" selects the 11.8*GHz* VCO (default state). The unused VCO is turned completely off in order to save power.

PLL2

The Secondary Phase Locked Loop (PLL2) is used for input reference clock "cleaning" in the forward-clocking mode or for output reference clock generation in the counter-clocking mode. It contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filtering capacitor of 47*nF* connected between the pins "ftr2p" and "ftr2n", and a ring VCO.

The operational modes of PLL2 are controlled by the external CMOS signals "oncc" and "offpll2". The default state for both signals is logic "1", which enables the counter-clocking mode for PLL1, but disables PLL2.

A logic "0" output CMOS loss-of-lock "lol2n" alarm signal is generated by PLL2 if its two input clock signals are not matching in phase and/or frequency.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. High-speed clock "C" is fed into the first divide-by-2 circuit that generates "C2". "C2" is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. "C16" ("offc64"=1, default) or "C64" ("offc64"=0) is passed on to a LVDS COB and becomes the output low speed clock signal "clo".

MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the "C16" clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a serial data stream running at a data rate up to 12.5*Gbps*. The latency of this circuit block is equal to roughly one period of the low-speed input clock. When "bitorder"=0 (default), "d00"is the MSB and when "bitorder"=1, "d15" is designated the MSB.

Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into the CML output signal "qcml" with a single ended swing of 600*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 12.5G*bps*.

HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 12.5*GHz* while producing a single-ended CML output swing of 600*mV*. The buffer can be enabled or disabled by the external 2-state control signal "offcho". The logic "0" state provides a full-rate clock output signal while the logic "1" state disables the buffer completely to save power.

LVDS COB x2

The dual LVDS Clock Output Buffer (LVDS COB x2) receives "cl" and "cc" signals and converts them into the LVDS output signals "clo" and "cco". Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Output Timing

Phase relation between the output data "qcml" and full rate output clock "cho" is specified in Table 1 and illustrated by Fig. 2.

Table 1. Output Data-to-Clock Phase Difference

Junction temperature, *°C*	**τ**, *ps*	
	Min.	Max.
-25	77	80
50	82	86
125	87	91

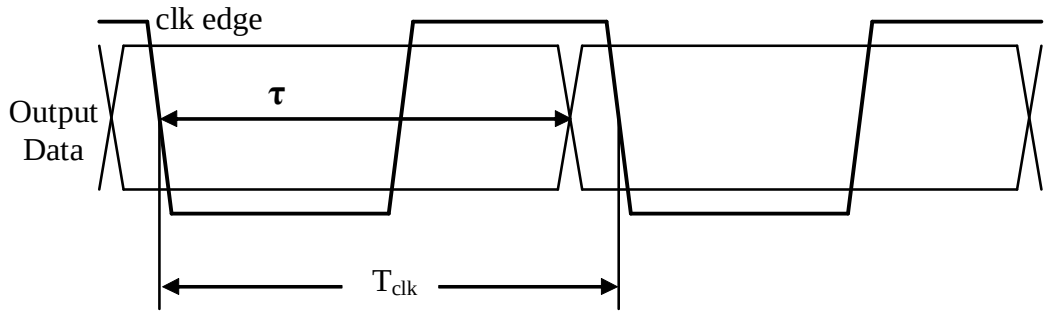

Fig. 2. Output Timing Diagram

TERMINAL FUNCTIONS

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
chop	33	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to "vcc". Can be disabled by "offcho".
chon	34		
qcmlp	39	Output	CML differential data outputs. Require external SE 50*Ohm* termination to "vcc".
qcmln	40		
Controls			
lol1n	19	LS Out, CMOS	PLL1 lock indicator (high: locked; low: no lock).
lol2n	52		PLL2 lock indicator (high: locked; low: no lock).
ftr1p	20	I/O	PLL1 external filter connection (1*nF* capacitor differential).
ftr1n	21		
ftr2p	54	I/O	PLL2 external filter connection (47*nF* capacitor differential).
ftr2n	53		
offecl	14	LS In., CMOS	LS input termination selector (active: low, CML or ECL depending on the "vecl" connection; default: high, LVDS).
offc64	16	LS In., CMOS	Division ratio clock selection (active: low, division by 64; default: high, division by 16).
offpll2	17	LS In., CMOS	PLL2 activation (active: low, PLL2 is enabled; default: high, PLL2 is disabled).
offcho	18	LS In., CMOS	HS COB control (active: high, buffer is disabled; default: low, full-rate output clock).
off12g	22	LS In., CMOS	VCO frequency selection (active: high, 11.0*GHz*; default: low, 11.8*GHz*).
oncc	31	LS In., CMOS	Counter clocking control (active: low, forward clocking mode; default: high, counter-clocking mode).
bitorder	59	LS In., CMOS	Input bit order selection (active: high, d15 is serialized first; default: low, d00 is serialized first).
Low-Speed I/Os			
cr16p	12	Input	Differential reference clock inputs with internal termination selectable through "offecl" and "vecl".
cr16n	13		
cdp	57	Input	Differential inputs for clock aligned with data. Internal termination is selectable through "offecl" and "vecl".
cdn	56		
clop	45	Output	LVDS clock outputs. Can transmit "C16" or "C64" divided clocks from PLL1 as defined by "offc64".
clon	46		
ccop	48	Output	LVDS clock outputs from PLL2.
ccon	49		
d00p	60	Input	
d00n	61		

d01p	63		Differential data inputs with internal termination selectable through “offecl” and “vecl”. Default is set to LVDS.
d01n	64		
d02p	66		
d02n	67		
d03p	69		
d03n	70		
d04p	72		
d04n	73		
d05p	77		
d05n	78		
d06p	80		
d06n	81		
d07p	83		
d07n	84		
d08p	86		
d08n	87		
d09p	89		
d09n	90		
d10p	92		
d10n	93		
d11p	95		
d11n	96		
d12p	98		
d12n	99		
d13p	3		
d13n	4		
d14p	6		
d14n	7		
d15p	9		
d15n	10		

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3*V*)	5, 8, 11, 25, 26, 29, 32, 35, 38, 41-44, 47, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100.
vee	Negative power supply. (GND or 0*V*)	1, 15, 23, 24, 30, 36, 50, 51, 75,
vecl	Input termination voltage. (“vcc” for CML, +2*V* for ECL)	2 and 74.
nc	Unconnected pin.	27, 28, 37, 58.

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
		General Parameters			
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
V_{ECL}		+2.0		*V*	
Power consumption		660		*mW*	
Junction temperature	-25	50	125	*°C*	
		LS Input Data (d00-d15)			
Data Rate	612.5		780	*Mbps*	
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
		LS Input Reference Clock (cr16, cd)			
Frequency	612.5		780	*MHz*	
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
		HS Output Data (qcml)			
Data Rate	9.8		12.5	*Gbps*	
Logic "1" level		V_{CC}		*V*	
Logic "0" level		V_{CC}-0.6		*V*	
Jitter		12		*ps*	Peak-to-peak at 12.5*Gb/s*
		HS Output Clock (cho)			
Frequency	9.8		12.5	*GHz*	
Logic "1" level		V_{CC}		*V*	
Logic "0" level		V_{CC}-0.6		*V*	
Jitter		6		*ps*	Peak-to-peak at 12.5*Gb/s*
Duty Cycle		50%			
		LS Output Clock (clo, cco)			
Frequency	612.5		780	*MHz*	
Interface		LVDS			Meets the IEEE Std.
		CMOS Control Inputs/Outputs			
Logic "1" level	V_{CC}-0.4			*V*	
Logic "0" level			V_{EE}+0.4	*V*	

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package's mechanical information is available on the company's website.